LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS)
Accredited by NAAC & NBA (Under Tier - I) and ISO 9001:2015 Certified Institution
Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.REDDY NAGAR, MYLAVARAM, KRISHNA DIST., A.P.-521 230.
http://www.lbrce.ac.in, Phone: 08659-222933, Fax: 08659-222931
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REPORT
on
AICTE Sponsored Online Short Term Training Program
"Mixed Signal Design Approaches for Artificial Intelligence Processors"
Series – 2 (1st February 2021 to 6th February 2021)

Department of ECE of Lakireddy Bali Reddy College of Engineering (Autonomous), has organized AICTE Sponsored Online Short Term Training Program (STTP) on "**Mixed Signal Design Approaches for Artificial Intelligence Processors**" under the coordinator ship of Dr. Srinivasulu Gundala. The Program was conducted as Series - 2 of three series scheduled from **01-02-2021 to 06-02-2021.**

ABOUT AICTE – STTP:

All India Council for Technical Education (AICTE) was set up in November 1945 as a national-level apex advisory body to conduct a survey on the facilities available for technical education and to promote development in the country in a coordinated and integrated manner. And to ensure the same, as stipulated in the National Policy of Education (1986), AICTE was vested with: Short Term Training Program (STTP) intends to conduct faculty trainings through financial assistance from AICTE to enable faculty members in the field of technical education to introspect and learn techniques that can help prepare students for active and successful participants in a knowledge society.

OBJECTIVES of STTP:

The objectives of the training program:

- To alleviate the Design and analysis of CMOS Mixed signal Circuits like current sources, Current and Voltage reference circuits, Voltage converters, and Data Converters of AI Processors,
- To design issues allied with high performance Mixed Signal designs.
- To provides platform to enhance the skills towards Design and development of intelligent computational systems for the Teaching faculty.

Date: 01st February 2021

Inauguration:

STTP was inaugurated on 1st February 2021 at 9:30 AM by **Dr. Y. Amar Babu** HOD of ECE and Convener of STTP along with chief guest of the programme **Mr. I. Balarama Krishnam Raju, HCL Technologies**, Principal of LBRCE **Dr. K. Appa Rao**, and Coordinator of STTP Dr. Srinivasulu Gundala.

Welcome to AICTE Sponsored Online Short Term Training Program on "Mixed Signal Design Approaches for Artificial Intelligence Processors"

Series – 2
1st February 2021 to 6th February 2021

Dr. Srinivasulu Gundala, has welcomed all the delegates and participants to the STTP. In his speech, he highlighted the main objectives and importance of this Short-Term Training Programme. Along with this, he gave a brief introduction about how the selection process has done.

Day 1: 1st Feb 2021 [FN]

Topic : DFT solutions for AI chips, Pipelined and High Speed ADC

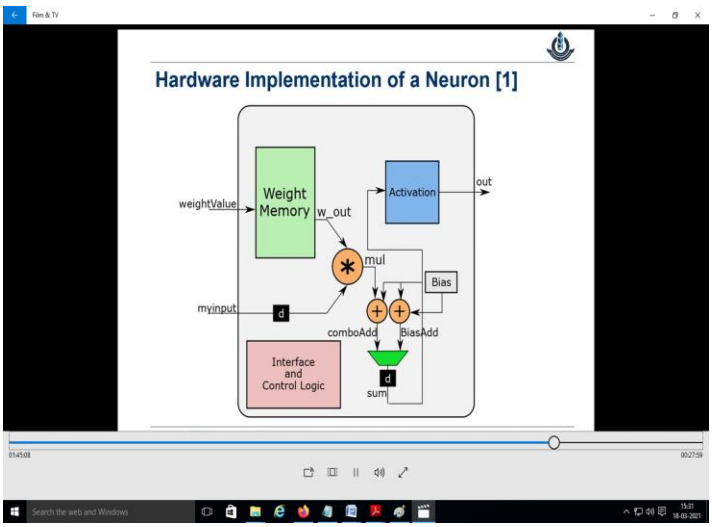
Resource Persons : Mr. I. Balarama Krishnam Raju, HCL Technologies
Dr. Jagadish D. N., Dept. of ECE, IIIT Dharwad

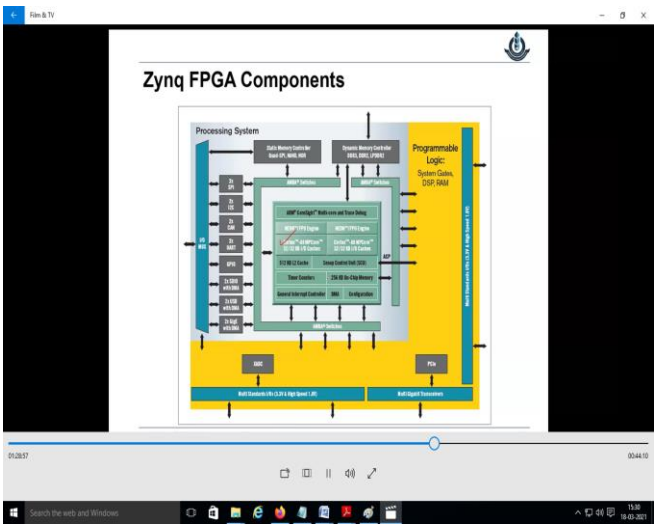
The resource Person, Mr. I. Balarama Krishnam Raju , started his lecture about the DFT solutions for AI chips and described and some key features of a design-for-test (DFT) strategy for AI chips, mentioned these three as top of them:

- Exploit AI chip regularity
- Insert and verify DFT at the RTL-level
- Improve the silicon bring-up flow

In his lecture he mentioned that the semiconductor companies are racing to develop AI-specific chips to meet the rapidly growing compute requirements for artificial intelligence (AI) systems. AI chips from companies like Graphcore and Mythic are ASICs based on the novel, massively parallel architectures that maximize data processing capabilities for AI workloads. Others, like Intel, Nvidia, and AMD, are optimizing existing architectures like GPU, CPU, and FPGA to keep up with the performance requirements of AI systems.

The resource Person, Dr. Jagadish D. N described about Pipelined and High Speed ADC, which has become the most popular ADC architecture for sampling rates from a few mega samples per second (Msps) up to 100Msps+. Resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. These resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (for example, HDTV), xDSL, cable modems, and fast Ethernet. Applications with lower sampling rates are still the domain of the successive approximation register (SAR) and integrating architectures, and more recently, oversampling/sigma-delta ADCs. The highest sampling rates (a few hundred Msps or higher) are still obtained using flash ADCs. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power in recent years.





Day 1: 1st Feb 2021 [AN]

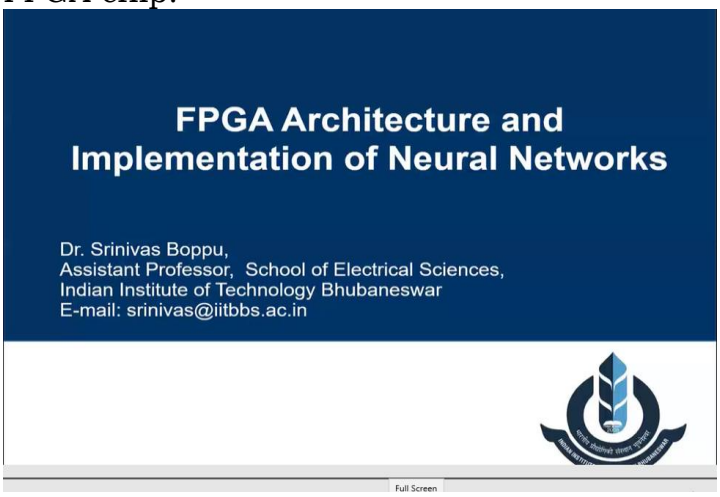
Topic : FPGA Architecture and Neural Networks Implementation

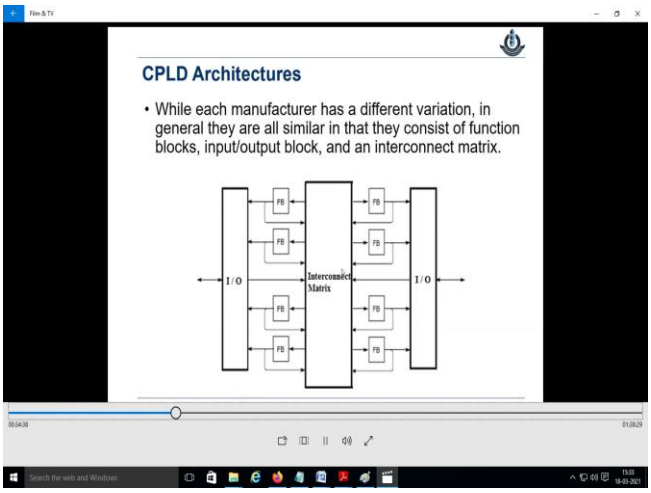
Resource Person : Dr. Srinivas Boppu, School of Electrical sciences, IIT Bhubaneswar

The resource Person, Dr. Srinivas Boppu has discussed about FPGA Architecture and Neural Networks Implementation. In his lecture he had elaborated the usage of the FPGA (Field Programmable Gate Array) for neural network

implementation which provides flexibility in programmable systems. He mentioned that the neural network based instrument prototype in real time application, conventional specific VLSI neural chip design suffers the limitation in time and cost. With low precision artificial neural network design, FPGAs have higher speed and smaller size for real time application than the VLSI design. In addition, artificial neural network based on FPGAs has fairly achieved with classification application. The programmability of reconfigurable FPGAs yields the availability of fast special purpose hardware for wide applications. Its programmability could set the conditions to explore new neural network algorithms and problems of a scale that would not be feasible with conventional processor.

The outcome of this lecture is to realize the hardware implementation of neural network using FPGAs. Digital system architecture is presented using Very High Speed Integrated Circuits Hardware Description Language (VHDL) and is implemented in FPGA chip.





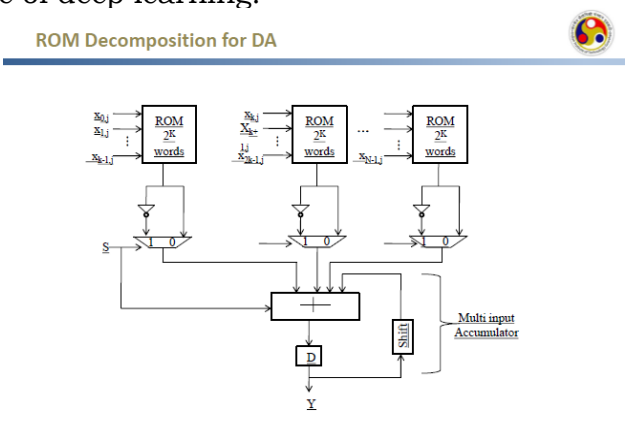
Day 2: 02nd Feb 2021 [FN]

Topics : Hardware Accelerators for Deep Learning.

Resource Person : Dr. Shaik Rafi Ahamed, Dept. of EEE, IITG, Guwahati.

The resource Person, Dr. Shaik Rafi Ahamed, started his lecture by giving a brief overview on Hardware Accelerators for Deep Learning. He explained that A deep learning processor (DLP), or a deep learning accelerator, is a specially designed circuitry optimized for deep learning algorithms, usually with separate data memory and dedicated instruction set architecture. Deep learning processors form a part of a wide range of today's commercial infrastructure, from mobile devices to cloud servers.

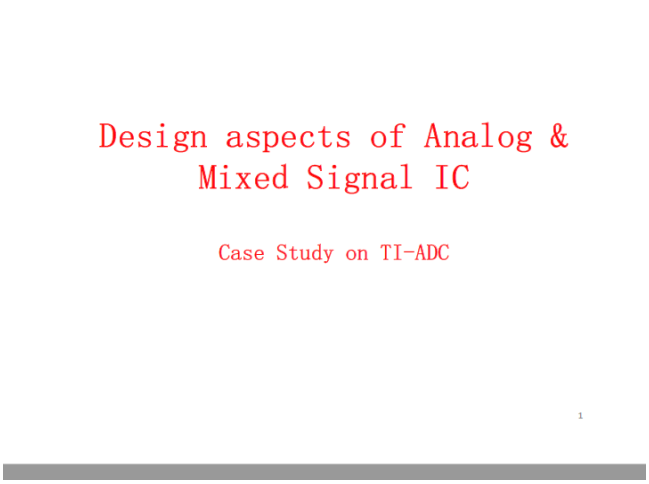
The conclusion of this lecture about DLPs is to provide higher efficiency and performance than existing processing devices, i.e., general CPUs (central processing units) and GPUs (graphics processing units), when processing deep learning algorithms. Just as GPUs are designed for graphic processing, DLPs leverage the domain-specific (deep learning) knowledge in designing architectures for deep learning processing. Commonly, most DLPs leverage a large number of computing components to leverage the high data-level parallelism, a relatively larger on-chip buffer/memory to leverage the data reuse patterns, and limited data-width operators to leverage the error-resilience of deep learning.

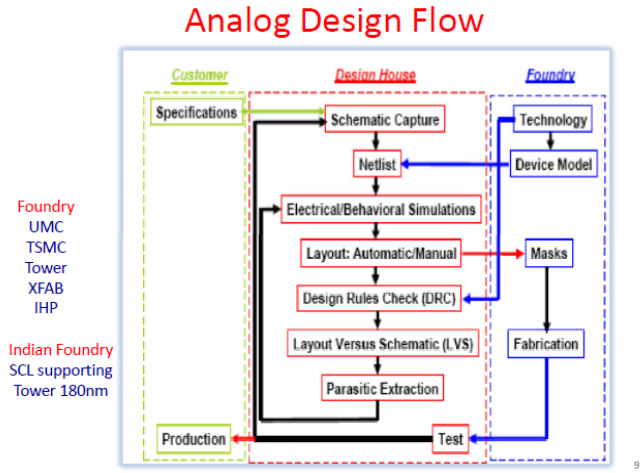


Day 2: 02nd Feb 2021 [AN]

Topics : Design and Characterization of High Speed ADCs.
Resource Person : Dr. Ankesh Jain, Dept. of Electrical Engg., IIT Delhi

The resource Person, Dr. Ankesh Jain given demonstration on Design and Characterization of High Speed ADCs. In his lecture he had given information to achieve wide dynamic range in high speed ADC applications, focused the need of attention must be given to the analog interface. Many ADCs are designed so that analog signals can be interfaced directly to their inputs without the necessity of a drive amplifier. This is especially true in ADCs such as the AD9220/21/23 family and the AD9042, where even a low distortion drive amplifier may result in some degradation in AC performance.

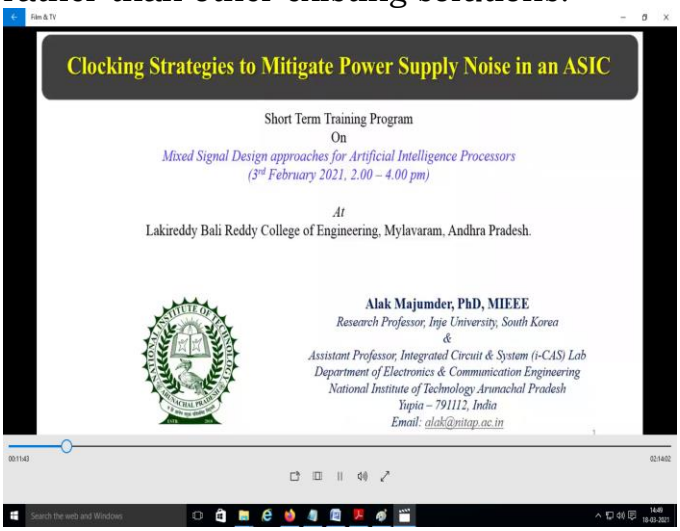


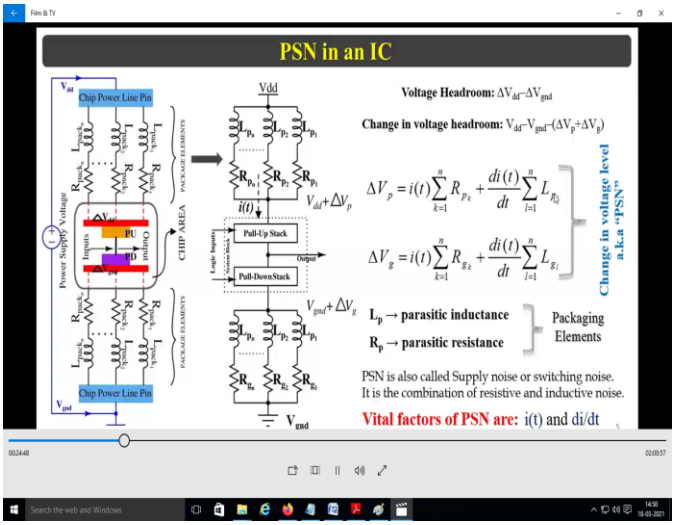


Day 3: 3rd Feb 2021 [FN]

Topics : Continuous Time Filter Design of AI Applications.
Resource Person : Dr. Krishna Lal Baishnab, Dept. of ECE, NIT, Silchar

The resource Person, Dr. Krishna Lal Baishnab has given lecture on Continuous Time Filter Design of AI Applications. In his lecture sir elaborated about the evolution of wireless applications i.e the performance as well as the number of users that has undergone tremendous growth in the last years, resulting in an increasing demand for smaller, low-cost wireless transceivers with low power consumption. In order to meet this demand, continuous development must take place both in CMOS technology and in RF electronics, the goal of which should be to achieve a fully-integrated single-chip receiver in a low-cost CMOS process. This demand for complex read channel and multi-standard receiver ICs calls for the design and implementation of one category of analog interface chips as continuous-time (CT) filters, suitable for high speed with variable bandwidths over a wide frequency range, preferably using the G_m-C approach rather than other existing solutions.



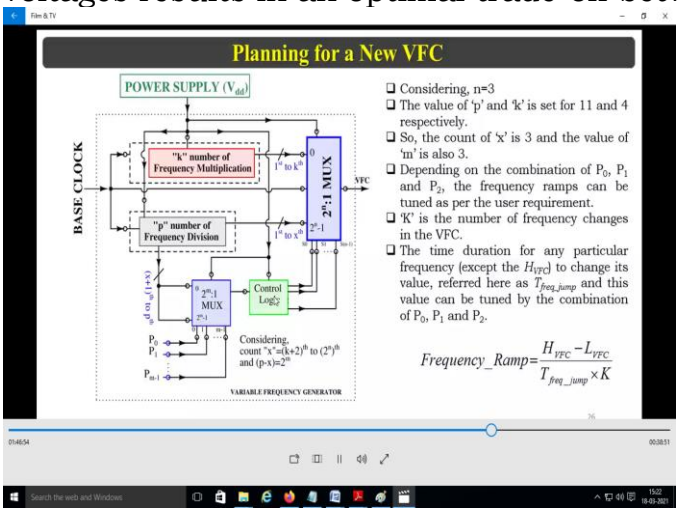


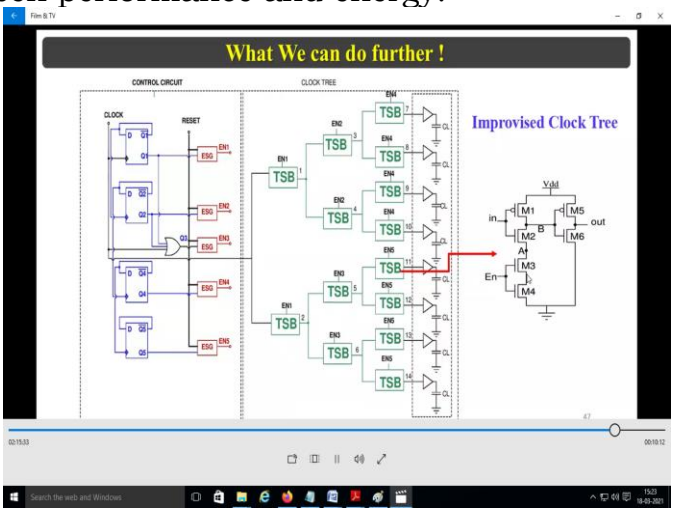
Day 3: 3rd Feb 2021 [AN]

Topic : Clocking Strategies for Supply Noise Mitigation in ASIC/AI processors.

Resource Person : Dr. Alak Majumder, Dept. of ECE, NIT Arunachal Pradesh

The resource Person, Dr. Alak Majumder has given lecture on Clock generation, and described about the distribution of clock in increased die size and increased number of cores in a microprocessor. Explored types of interrelated works: 1) analytical modeling of period jitter of global clock distribution induced by power supply droop, 2) circuit design of a power supply droop detector with 20mV resolution and 1 cycle latency, and 3) architectural studies regarding new adaptive clocking architectures which reduce the worst case period jitter and the worst timing slack. Demonstrated test-chip capable of characterizing spatial variation in digital circuits is developed and implemented in a 90nm triple-well CMOS process. Highlighted the importance of adaptive body-biasing and voltage scaling as variation mitigation techniques proves voltage scaling is more effective in performance modification with reduced impact to idle power compared to body-biasing. Finally, the addition of power-supply voltages in a massively parallel multi core processor is explored to reduce the energy required to cope with process variation. An analytic optimization framework is developed and analyzed; using a custom simulation methodology, total energy of a hypothetical 1K-core processor based on the RAW core is reduced by 6-16% with the addition of only a single voltage. Analysis of yield versus required energy demonstrates that a combination of disabling poor-performing cores and additional power-supply voltages results in an optimal trade-off between performance and energy.



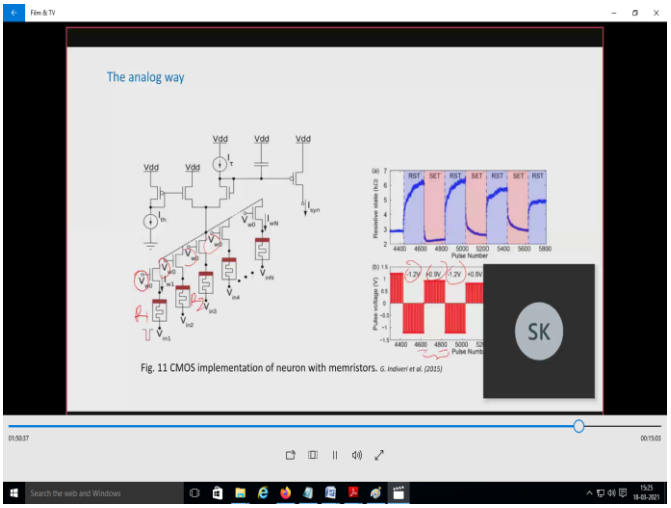


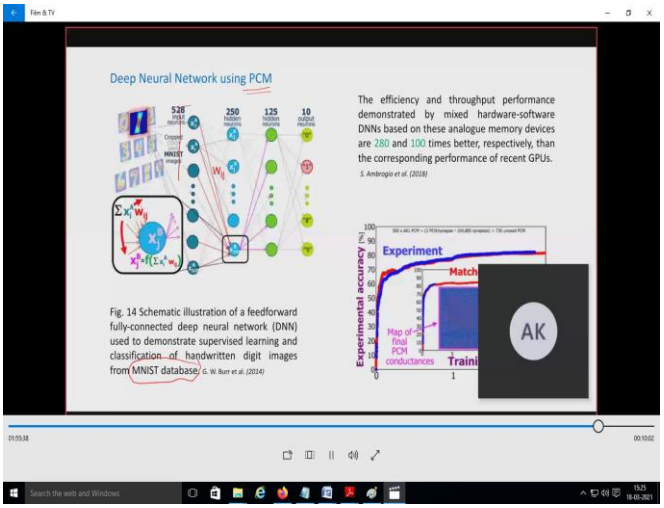
Day 4: 4th Feb 2021 [FN]

Topics: Hardware for Artificial Neural Networks and Brain Inspired Computing.

Resource Person: Dr. Sakthivel R, SELECT, VIT, Vellore

The resource person Dr. Sakthivel R. elaborated on Hardware for Artificial Neural Networks and Brain Inspired Computing. In his lecture he described that the next generation of high-performance, low-power computer systems might be inspired by the brain. However, as designers move away from conventional computer technology towards brain-inspired (Neuromorphic) systems, they must also move away from the established formal hierarchy that underpins conventional machines — that is, the abstract framework that broadly defines how soft-ware is processed by a digital computer and converted into operations that run on the machine's hardware. This hierarchy has helped enable the rapid growth in computer performance. Future developments in artificial intelligence will profit from the existence of novel, non-traditional substrates for brain-inspired computing. Neuromorphic computers aim to provide such a substrate that reproduces the brain's capabilities in terms of adaptive, low-power information processing.



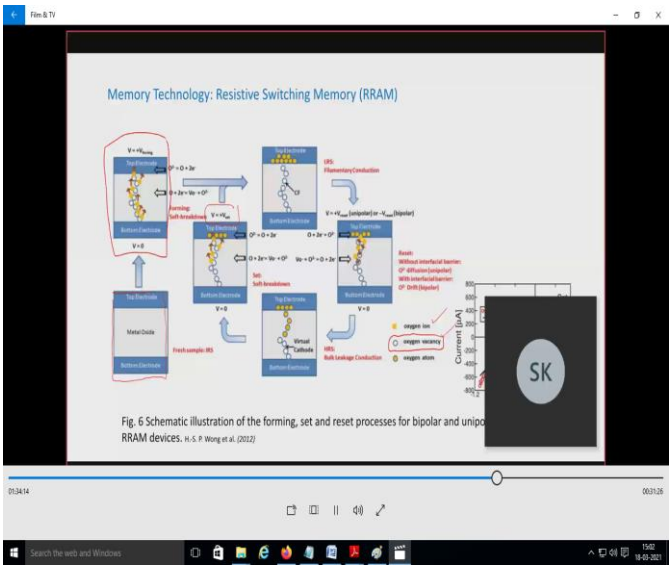


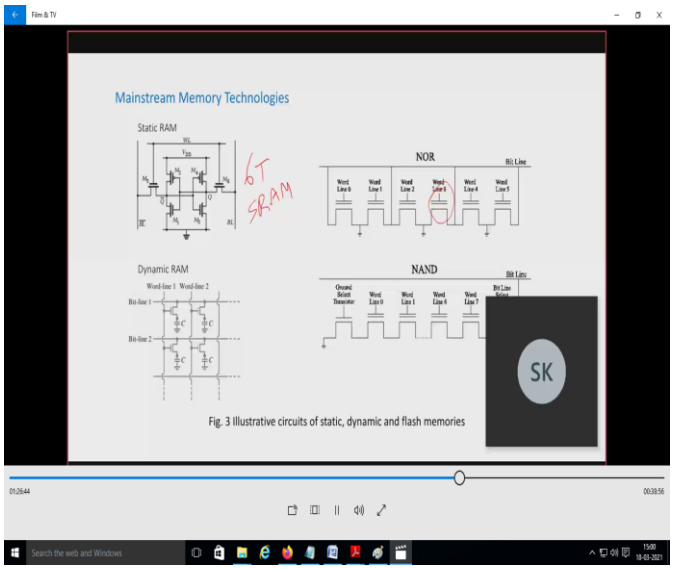
<u>Day 4: 4th Feb 2021 [AN]</u>

Topics : Introduction to Neuromorphic Computing

Resource Person : Dr. Jagadish D. N., Dept. of ECE, IIIT Dharwad

The resource person Dr. Jagadish D. N given his lecture on Introduction to Neuromorphic Computing. In his lecture he described Neuromorphic computing is an emerging field that has the potential to drastically influence every human's life within the next decades. Neuromorphic computing explores the computing process of the brain and attempts to replicate it onto modern electronics. It offers improvements on current computer architecture, von Neumann architecture, and will lead to more efficient computing, easier development of machine learning, and further integration of electronics and biology. Neuromorphic computing has come to refer to a variety of brain-inspired computers, devices, and models that contrast the pervasive von Neumann computer architecture. This biologically inspired approach has created highly connected synthetic neurons and synapses that can be used to model neuroscience theories as well as solve challenging machine learning problems. The promise of the technology is to create a brain-like ability to learn and adapt, but the technical challenges are significant, starting with an accurate neuroscience model of how the brain works, to finding materials and engineering breakthroughs to build devices to support these models, to creating a programming framework so the systems can learn, to creating applications with brain-like capabilities.



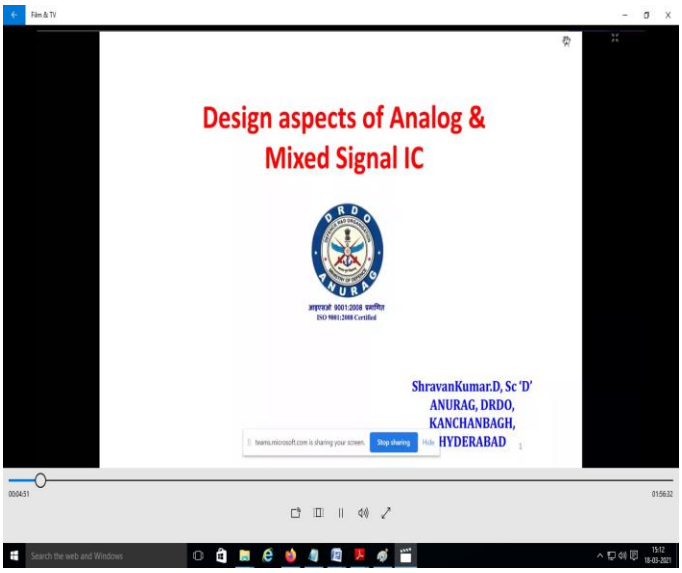


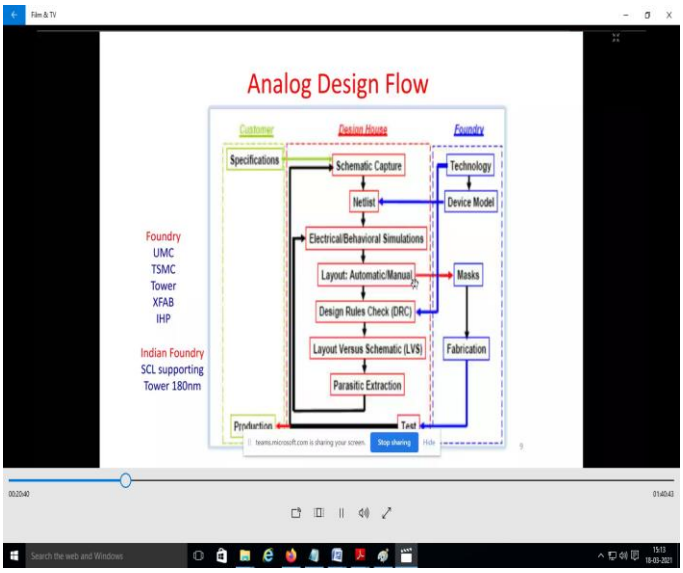
Day 5: 5th Feb 2021[FN]

Topics : **Role of Emerging Non-volatile Memories in AI**

Resource Person : **Dr. M. Hasan, Dept. of Electronics Engineering, AMU, Aligarh**

The resource Person, Dr. M. Hasan has explained about the Role of Emerging Non-volatile Memories in Artificial Intelligence. Emerging nonvolatile memory technologies such as magnetic random-access memory (MRAM), spin-transfer torque random-access memory (STT-RAM), ferroelectric random-access memory (FeRAM), phase-change memory (PCM), and resistive random-access memory (RRAM) combine the speed of static random-access memory (SRAM), the density of dynamic random-access memory (DRAM), and the nonvolatility of Flash memory and so become very attractive as another possibility for future memory hierarchies. Many other new classes of emerging memory technologies such as transparent and plastic, three-dimensional (3-D), and quantum dot memory technologies have also gained tremendous popularity in recent years. Subsequently, not an exaggeration to say that computer memory could soon earn the ultimate commercial validation for commercial scale-up and production the cheap plastic knockoff. Therefore, this review is devoted to the rapidly developing new class of memory technologies and scaling of scientific procedures based on an investigation of recent progress in advanced Flash memory devices.





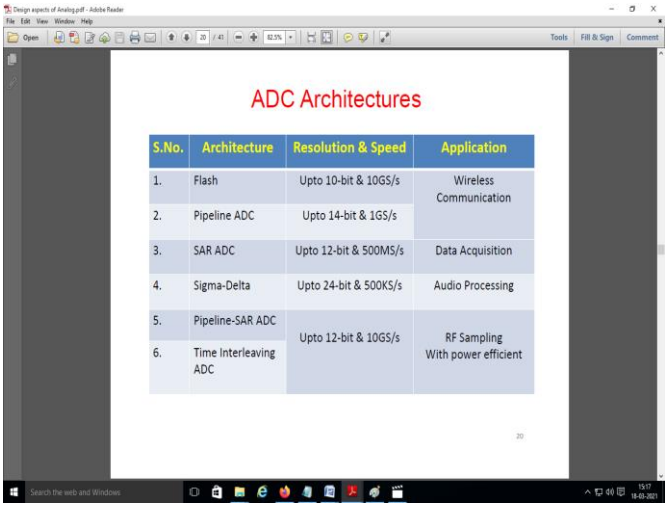
Day 5: 5th Feb 2021[AN]

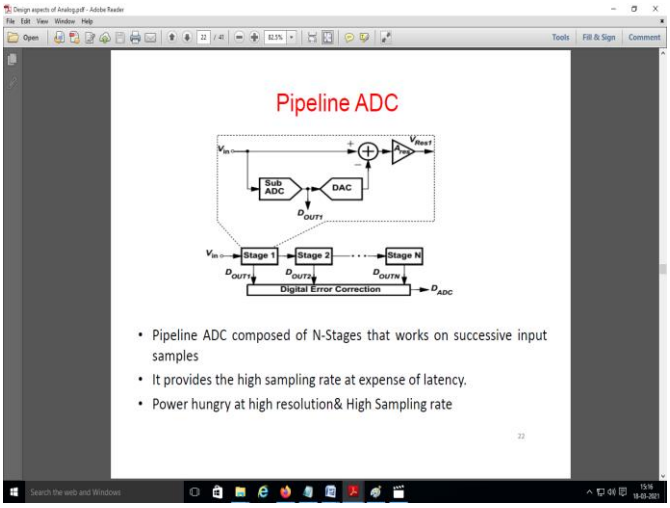
Topic : **Design aspects of Analog and Mixed signal IC and Case studies on ADC.**

Resource Person : Dr. Shravankumar Donthula, RCIL, DRDO, Hyderabad

The resource Person Dr. Shravankumar Donthula, RCIL, DRDO, Hyderabad given his lecture on the Design aspects of Analog and Mixed signal IC and Case studies on ADC. Explore how a Crosstalk can be minimized in mixed-signal System-on-Chip (SoC), i.e., when analog and digital circuits are integrated on the same silicon chip, performance limitations come mainly from the analog section which interfaces the digital processing core with the external world. In such ICs, the digital switching activity may affect the analog section. Increasing pressure on production costs and, more generally, time to market, have impacted all levels of IC design. In this context, one of the major challenges is to avoid silicon failure or yield loss. Indeed, a widely accepted statistic today is that almost half of all designs fail at first silicon. Failure costs are obviously due to new mask generations, and additional engineering time, but also to the potential miss of a large part of the market window for a

product. Therefore, first-pass silicon success and high design yield has become a fundamental requirement for IC designs, and is, quite naturally, driving an increasing need for integrated circuit verification and debugging solutions to use appropriate CAD solutions for design a high-resolution ADC. Suggested to consider three different design levels-Modeling, Architectural design, and Physical design.



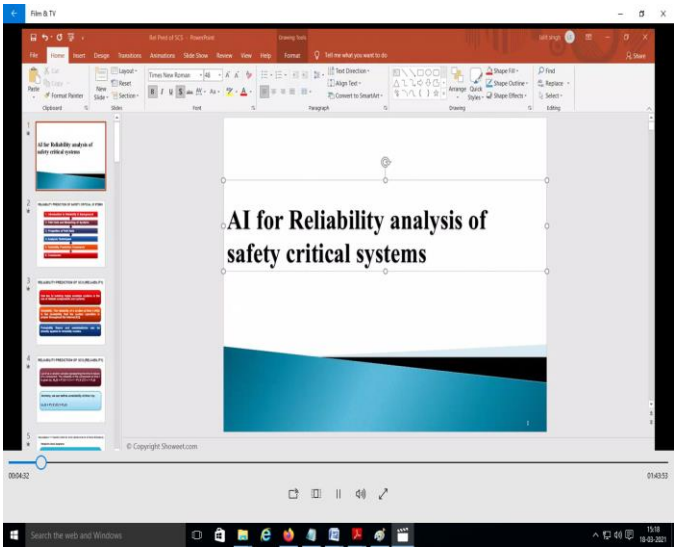


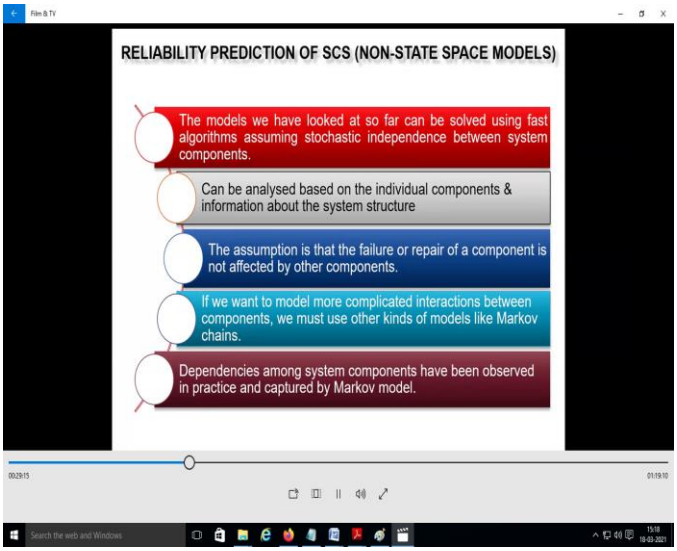
Day 6: 6th Feb 2021[FN]

Topic : **AI for Reliability Analysis of Safety Critical Systems**

Resource Person : **Dr. Lalith Singh, BARC, Govt. of India**

The resource Person Dr. Lalith Singh, BARC, Govt. of India given lecture on Artificial Intelligence (AI) for Reliability Analysis of Safety Critical Systems. In his lecture he explained about safety-critical autonomous systems are becoming more powerful and more integrated to enable higher-level functionality. Modern multi-core SOCs are often the computing backbone in such systems for which safety and associated certification tasks are one of the key challenges, which can become more costly and difficult to achieve. Hence, modelling and assessment of these systems can be a formidable task. In addition, Artificial Intelligence (AI) is already being deployed in safety critical autonomous systems and Machine Learning (ML) enables the achievement of tasks in a cost-effective way. Compliance to Soft Error Rate (SER) requirements is an important element to be successful in these markets. When considering SER performance for functional safety, we need to focus on accurately modeling vulnerability factors for transient analysis based on AI and Deep Learning workloads. The reliability risks due to these new use cases also need to be comprehended for modeling and mitigation and would directly impact the safety analysis for these systems.



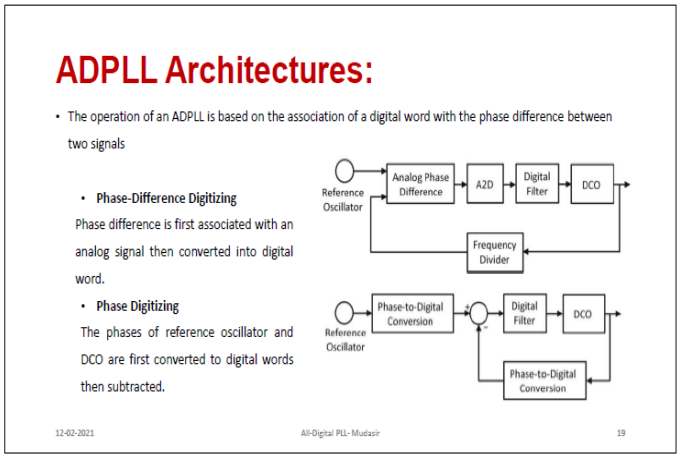


Day 6: 6th Feb 2021[AN]

Topic : Digital Phase Locked Loops-Design Approaches

Resource Person : Dr. Mudasir Bashir, Infineon Technologies, Austria

The resource Person Dr. Mudasir Bashir, Infineon Technologies, Austria given his lecture on Digital Phase Locked Loops-Design Approaches, in his lecture he describes that Phase Locked Loop (PLL) is a feedback system that is configured as frequency multipliers, tracking generators, demodulators and clock recovery circuits. He explained about today the most challenging requirement engineers' face is design of fast locking PLL with low jitter. Many analog techniques are proposed to fulfill the demand but they result in increasing complexity of design and long lock in time. A detailed analysis of various techniques for designing the phase detector, digital loop filter and digital controlled oscillator in ADPLL is provided. Among all the methods to design detector, PFD with TDC is the best approach as the amount of glitches using this method is less. Digital loop filter is designed using bilinear transformation of RC loop filter. DCO structure based on ring oscillator is preferred for low power and low complex design. Finally, if we use PFD, TDC and digital loop filter together in ADPLL, various parameters such as lock-in time, power consumption and stability can be evaluated and comparison with the results of existing ADPLL structures can be carried out.



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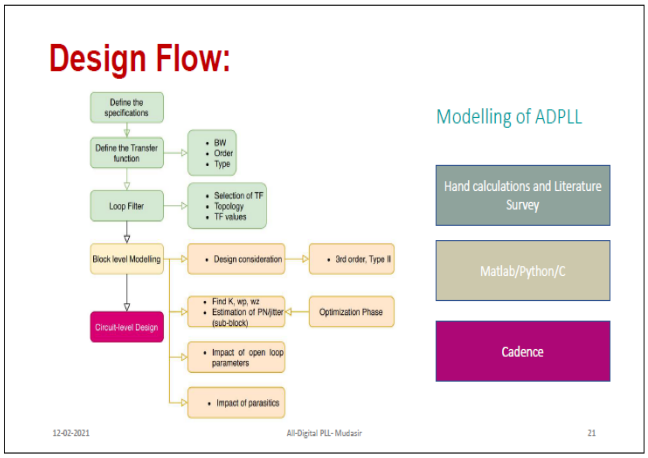

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Date: 06th Feb 2021: Valedictory Session:

STTP Valedictory Session held on 06th February 2021 at 3:45 PM by Coordinator of STTP **Dr. Srinivasulu Gundala,** Convener of STTP **Dr. Y. Amar Babu** along with Principal of LBRCE **Dr. K. Appa Rao,** chief guest of the programme **Dr. Mudasir Bashir,** Infineon Technologies, Austria, and Participants. Dr. K. Appa **Rao** in his valedictory addressing, conveyed his wishes to all the participants of STTP, congratulated the Program Convener Dr. Y. Amar Babu and Coordinator Dr. Srinivasulu Gundala for organizing the STTP in a successful manner. Further, he appreciated all the Teaching and Non-Teaching Staff Members of ECE department for promoting such kind of development programme. He also motivated to keep learning new technologies coming in future for the career growth as well as organizational growth.

At the end of the valedictory session, vote of thanks was given by **Dr. Srinivasulu Gundala, Coordinator of the STTP** in which he has been paid his gratitude to AICTE for sponsoring the STTP program, resource persons for spending valuable time for our participants and sharing the knowledge and all the participants for attending this STTP.

Expressed the gratitude to the **LBRCE management**, Principal **Dr. K. Appa Rao,** Dean R & D **Dr. E. V. Krishna Rao** and team, Teaching and non-teaching staff members of ECE dept. and Microsoft Teams online software providers for extending support and for providing us with an environment to complete STTP program successfully.

Feedback from the Participants:

The feedback of the participants was very positive and motivational for the organizers. The participants felt very happy for conducting the STTP on latest trends in Industry. They said that, this program was very useful and helpful for them in their research, in turn guiding students in latest technologies. All the participants appreciated the sessions organized by the department of ECE and the arrangements made by the organizers.

The number of Online registrations by the Faculty of AICTE approved institutions and Research scholars were 100 for Series- 2, on an average 79 participants participated in online sessions, based on the eligibility criteria of the AICTE norms, the e-certificates were issued to 64 participants.

12.02.2021

Coordinator
(Dr. Srinivasulu Gundala)

Convener
(Dr. Y. Amar Babu)