



LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS)
Accredited by NAAC & NBA (Under Tier - I) and ISO 9001:2015 Certified Institution Approved
by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.REDDY NAGAR, MYLAVARAM, KRISHNA DIST., A.P.-521 230.
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

REPORT

on

Faculty Development Program (FDP) “Design and Implementation of advanced VLSI Architectures” (13.03.2023 to 17.03.2023)

Department of ECE of Lakireddy Bali Reddy College of Engineering (Autonomous), has organized FDP on “Design and Implementation of advanced VLSI Architectures” under the coordinator-ship of Dr. Srinivasulu Gundala. The Program was conducted from **13-03-2023 to 17-03-2023**.

OBJECTIVES of FDP:

The objectives of the training program are:

- To provide knowledge of Efficient VLSI Hardware Design for AI&ML, NoC Architectures & FPGA Implementation.
- To inculcate Research ideas on RF IC Design.
- It provides platform to enhance the skills towards Design Strategies for Applications & Challenges in Modern era VLSI.

OUTCOMES of FDP:

- Design of VLSI Architectures for Wireless applications.
- Development of NoC Architectures and Implementation on FPGA.
- Implementation of Algorithms and Circuit minimization techniques.

Date: 13th March 2023

Inauguration:

FDP was inaugurated on 13th March 2023 at 1:30 PM by **Dr. Y. Amar Babu**, HOD of ECE and Convener of FDP along with chief guest of the programme **Dr. Rakesh Kumar Palani**, Professor, IIT Delhi, Principal of LBRCE **Dr. K. Appa Rao**, and Coordinator of FDP **Dr. Srinivasulu Gundala**.



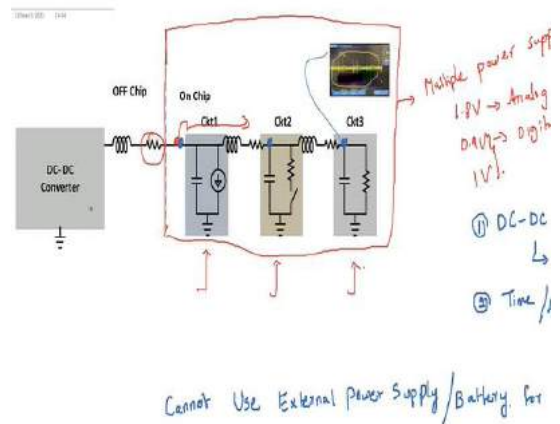
Dr. Srinivasulu Gundala, has welcomed all the delegates and participants to the FDP. In his speech, he highlighted the main objectives and importance of this FDP. Along with this, he gave a brief introduction about eligibility for awarding the certificate.

Day 1: 13th March 2023

Topic : Systematic Design of Band gap Circuits

Resource Person : Dr. Rakesh Kumar Palani, Professor, Dept. of Electrical Engineering, IIT Delhi

Dr. Rakesh Kumar Palani, Professor, Dept. of Electrical Engineering, IIT Delhi started his presentation on voltage difference between two p-n junctions, operated at different current densities, is used to generate a current that is in a resistor for making band gap circuits. This current is used to generate a voltage in a second resistor. This voltage in turn is added to the voltage of one of the junctions. The remaining voltage change over the operating temperature of typical integrated circuits is on the order of a few milli volts. This temperature dependency has a typical parabolic residual behavior since the linear (first order) effects are chosen to cancel. Therefore, recent work concentrates on finding alternative solutions, in which for example currents are summed instead of voltages, resulting in a lower theoretical limit for the operating voltage.



Day 2: 14th March 2023

Topics : Efficient VLSI Hardware Design for AI&ML.

Resource Person : Dr. Sakthivel R, Professor, VIT Vellore

The resource Person Dr. Sakthivel R., School of Electronics Engineering, VIT Vellore, explored insights of Artificial intelligence methods used in different interdisciplinary areas. The method of machine learning and data mining for testing and fault diagnostics in analog/mixed-signal integrated circuits. The case study results for analog filters are demonstrated and discussed. The proposed method and approach can be used according to the design-for-testability flow for analog/mixed-signal integrated circuits.



Brain Inspired Vs Von-Neumann Computing

• Human brain

parallel architecture	analog
10^{11} neurons	10 Hz
10^{15} synapses	20 W

Simulations of mouse cortex on Blue Gene L

Von-Neumann architecture	digital
$8 \cdot 10^4$ neurons	1 GHz
$5 \cdot 10^{10}$ synapses	40 kW

super-computers slower than mouse ($\times 10$)

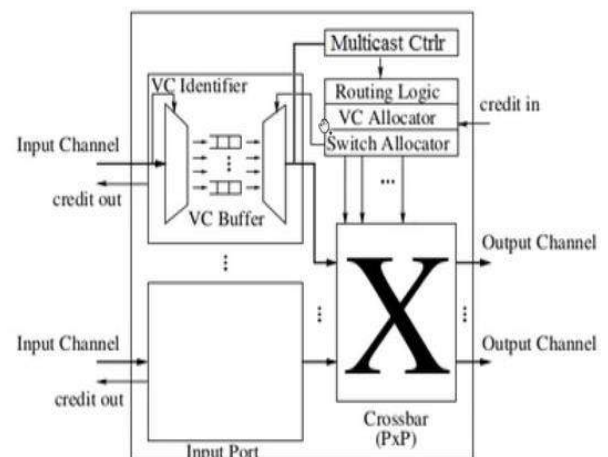
	IBM TrueNorth	Human brain	Gap
Number of cores	4096		
Number of neurons	10^6	0.86×10^{11}	$\sim 10^5$

Day 3: 15th March 2023

Topics : NoC Architectures and FPGA Implementation

Resource Person : Dr. B. Naresh Kumar Reddy, Professor, NIT Trichy

The resource Person Dr. B. Naresh Kumar Reddy, Professor, NIT Trichy, started his demonstration by giving today's NoC architectures and FPGA systems have reached the heights not expected by human being. Networks-on-chip constitute an emerging technology for systems-on-chip, which can benefit significantly from the techniques of network systems architecture, more specifically from switching architectures. Architectural and circuit design methods are critical in the design and evaluation of NoC architectures, considering the strong dependency of NoCs on implementation technology and the requirements of NoC architectures for high performance in addition to low power consumption. He presented the main technological challenges of NoC architectures and a circuit analysis of NoC architectures using VLSI models, taking into account the interaction of network structure and implementation technology.

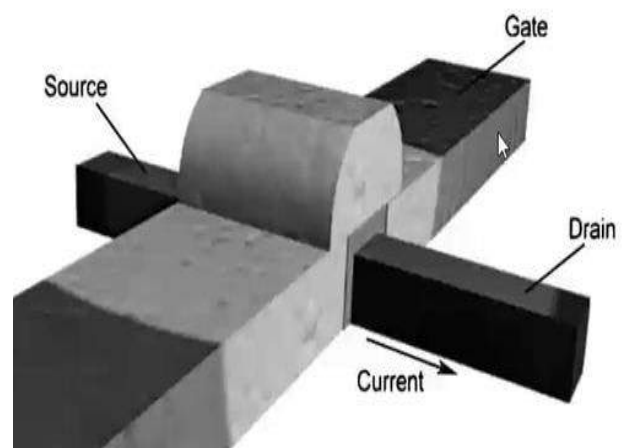


Day 4: 16th March 2023

Topics : Device and Circuit Modelling

Resource Person : Dr. Gopi Krishna Saramakala, Professor, NIT Calicut

The resource Person Dr. Gopi Krishna Saramakala, Professor, NIT Calicut, explored insights of device model is a analytical expression developed on experimental and theoretical study. Variables & constants that make-up this Analytical-Expression are based on model parameters. In contrary, device parameters are used to reproduce the actual device characteristics on a simulator. The case study results for analog filters are demonstrated and discussed. The proposed method and approach can be used according to the design-for-testability flow for analog/mixed-signal integrated circuits

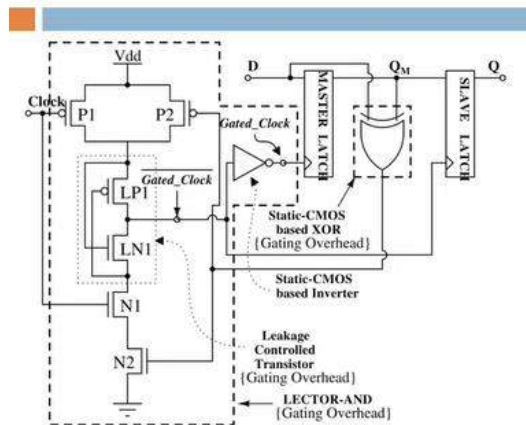


Day 5: 17th March 2023

Topics : Design Strategies for Low-Power IC

Resource Person : Dr. Alak Majumder, Professor, NIT Arunachal Pradesh

The resource Person Dr. Alak Majumder, Professor, NIT Arunachal Pradesh, explored insights of Design Strategies for Low-Power IC. He highlighted the advantage of utilizing low-power components in conjunction with low area design techniques. Requirements for “Lower power consumption continue” to increase as components become battery-powered, smaller and more functionality. The motivations for reducing power consumption application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation.



Date 5: 17th March 2023:

FDP Valedictory Session held on 17th March 2023 at 2:20Pm by Coordinator of FDP **Dr. Srinivasulu Gundala**, Convener of FDP **Dr. Y. Amar Babu** along with Dean R & D of LBRCE **Dr. E.V. Krishna Rao**, chief guest of the programme **Dr. Alak Majumder, Professor, NIT Arunachal Pradesh** and Participants.

Dr. Dr. E.V. Krishna Rao in his valedictory addressing, conveyed his wishes to all the participants of FDP. Further, he appreciated all the Teaching and Non-Teaching Staff Members of ECE Department for promoting such kind of development programme. He also motivated to keep learning new technologies coming in future for the career growth as well as organizational growth. Coordinator of the FDP in which he has been paid his gratitude to LBRCE Principal and Management for sponsoring the FDP program, Resource persons for their valuable time..

Expressed the gratitude to the LBRCE management, Principal Dr. K. Appa Rao, Dean R & D Dr. E. V. Krishna Rao and team, Teaching and non-teaching staff members of ECE dept. and Microsoft Teams online software providers for extending support and for providing us with an environment to complete FDP program successfully.

Feedback from the Participants:

The feedback of the participants was very positive and motivational for the organizers. The participants felt very happy for conducting the FDP on latest trends in Industry. All the participants appreciated the sessions organized by the department of ECE and the arrangements made by the organizers. The number of Online registrations by the Faculty members and Research scholars of AICTE approved institutions were 205, on an average 144 participants participated in online sessions and e-certificates were issued to participants.

19.03.2023



Coordinator
(Dr. Srinivasulu Gundala)



Convener
(Dr. Y. Amar Babu)



5 Day FDP Program Schedule of



Design and Implementation of Advanced VLSI Architectures

13.03.2023

14.03.2023

15.03.2023



**Dr. Rakesh Kumar Palani,
Professor, IIT Delhi**

Topic

**Systematic Design of
Bandgap Circuits**



**Dr. Sakthivel R,
Professor, VIT Vellore**

Topic

**Efficient VLSI Hardware
Design for AI&ML**



**Dr. B. Naresh Kumar Reddy,
Professor, NIT Trichy**

Topic

**NoC Architectures and
FPGA Implementation**

16.03.2023

17.03.2023



**Dr. Gopi Krishna Saramakala,
Professor, NIT Calicut**

Topic

Device and Circuit Modelling



**Dr. Alak Majumder, Professor,
NIT Arunachal Pradesh**

Topic

Design Strategies for Low-Power IC

**Valedictory Program on
17.03.2023@ 03:50PM**

**Organized by
Dept. of ECE, Lakireddy Bali Reddy College of Engineering (Autonomous)
L. B. Reddy Nagar, Mylavaram-521 230, NTR (Dt.), A.P.**



About the Institute

The Lakireddy Bali Reddy College of Engineering (LBRCE), Mylavaram was established in the year 1998 by Lakireddy Bali Reddy Charitable Trust, whose architect is Er. Lakireddy Bali Reddy garu. It is approved by AICTE, affiliated to JNTUK, Kakinada and attained autonomous status in the year 2010. It is accredited with NAAC and NBA (CSE, IT, ECE, EEE & ME) under Tier-I. Offering 9 B.Tech programs, 4 M.Tech programs and M.B.A.



About the Department

The Department of Electronics & Communication Engineering was started in the year 1998. The Department is accredited by NBA (Tier-I). It is recognized as a Research centre by JNTUK Kakinada. Received sponsored projects worth of Rs.1.5 crore from reputed R&D agencies.

Resource Persons



Dr. Rakesh Kumar Palani,
Professor, IIT Delhi



Dr. B. Naresh Kumar Reddy,
Professor, NIT Trichy



Dr. Gopi Krishna Saramakala,
Professor, NIT Calicut



Dr. Alak Majumder, Professor,
NIT Arunachal Pradesh



Dr. Sakthivel R,
Professor, VIT Vellore

**Online
mode**

No Registration FEE

REGISTRATION LINK

<https://tinyurl.com/LBRCE-FDPDIVLSIA>

Last date for Registration: 10-03-2023

Chief Patrons

(Late) Shri. L. Bali Reddy, Founder Chairman.
Shri. L. Jaya Prakash Reddy, Co-Founder & Honorary-Chairman.
Shri. L. R. N. K. Prasad Reddy, Chairman.

Patrons

Shri. G. Srinivasa Reddy, President, LBCT.
Dr. K. Appa Rao, Principal.
Dr. K. Harinadha Reddy, Vice-Principal.

Convener

Dr. Y. Amar Babu, Ph. D
HOD ECE, LBRCE

Coordinator

Dr. Srinivasulu Gundala, Professor,
9440831750

Co-coordinators

Mr. Venkata Rao G., Associate Professor,
949535698
Mr. Dharmachari N., Assistant Professor,
9885881557

FDP Objectives

- To provide knowledge of Efficient VLSI Hardware Design for AI&ML, NoC Architectures & FPGA Implementation.
- To inculcate Research ideas on RF IC Design.
- It provides platform to enhance the skills towards Design Strategies for Applications & Challenges in Modern era VLSI.

FDP Outcomes

- Design of VLSI Architectures for Wireless applications.
- Development of NoC Architectures and Implementation on FPGA.
- Implementation of Algorithms and Circuit minimization techniques.

Faculty Development Programme on Design and Implementation of Advanced VLSI Architectures

13.03.2023 TO 17.03.2023
2.00 PM TO 4.00PM

Contents of FDP

- Efficient VLSI Hardware Design for AI&ML
- NoC Architectures and FPGA Implementation
- Systematic Design of Bandgap Circuits
- Design Strategies for Low-Power IC
- Applications and Challenges in Modern era VLSI

Organized By

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