LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING
(Autonomous Status Since the Academic Year 2010-11 & Extended up to 2031-32)
NAAC Accredited with CGPA of 3.20 on 4-point scale at 'A' Grade
NIRF-2022 (Positioned in the Band of 251-300 in the Engineering Category)
NIRF-2023 (Positioned in the Band of 101-150 in the Innovation Category)
NBA Accredited under Tier-I (ECE, EEE, CSE, IT, ME, CIV, ASE)
Recognized as Scientific Industrial Research Organization(SIRO) by DSIR
Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.Reddy Nagar, Mylavaram-521230, N.T.R Dist., Andhra Pradesh, India.
Department of Electronics and Communication Engineering

Report on one-week Hands-On Training Program on "VLSI Universal Verification Methodology"

Event Type	:	Hands-On Training program
Date / Duration	:	03rd March 2025 to 08th March 2025
Resource Person	:	Mr. Venkatesh Raja Kutti, TARAS Systems and Solutions
Name of Coordinator(s)	:	Dr .B. Rambabu
Name of Co-Coordinator(s)	:	Mrs. T. Kalpana, Mrs. K. Balavani
Target Audience	:	VI Semester B. Tech Students
Total no of Participants	:	VI Semester B. Tech Students - 68 Nos.
Objective of the event	:	It provides platform to enhance the skills towards Design Strategies for Applications & Challenges in Modern era VLSI.
Outcome of event	:	By attending this training program , the students can be able to learn the advances in VLSI. Gaining Knowledge on System Verilog and Universal Verification Methodology (UVM) for VLSI UVM. Learns the essential skills and knowledge needed to succeed in a hardware design and verification domain.

Description / Report on Event:

Training Program was inaugurated on 03rd March 2025 at 9:00 AM by **Dr. G. Srinivasulu**, **HOD** of ECE and Coordinator **Dr. B. Rambabu** with the resource person of the program as **Mr**. **Venkatesh Raja Kutti**. The Hands - On training on VLSI UVM is conducted for one week to VI semester B. Tech ECE students.

Dr. G. Srinivasulu, **Head,** Department of ECE , who highlighted the significance of the training. It was mentioned that with the technology evolving faster the students should always update themselves with the current trends. Irrespective of running behind non-core jobs, students need to strength their core concepts and opt for a better carrier that is consistent**.** Mrs. T. Kalpana and Mrs. K. Balavani coordinated the training.

Day 1 has begun with explanation about the basics of Verilog and system Verilog by the resource person Mr. Venkatesh Raja Kutti from "TARAS Systems and Solutions" The objective of this training program is to educate the students about the VLSI environment. As these are the days of verification in majority of the applications, knowledge about programming using Verilog, System Verilog and Universal Verification Methodology (UVM) will enable in providing verification results. Once the basic concepts were introduced, code is written for Full Adder , demultiplexer and the same is executed in EDA Playground and verified results. Along with this few interview questions also discussed on Verilog and System Verilog.

Day 2 The resource Person delivers the insights about the features of System Verilog, its data types, System Verilog constraints, Verilog testbench development and exercised the programs based on two state and four state data types, arrays and different class methods. Introduction to UVM, history of verification methodology, verification Challenges in test bench and design requirements, UVM class library and UVM object, macros and Practical programs on UVM class library.

Day 3 the resource person explains every component in the UVM test bench and also explained the importance of inheritance concept. Mainly focused on Transaction Level Modelling (TLM) port, which is used to connect two components and also explained about inbuilt libraries in UVM. Along with this few interview questions also discussed on UVM.

Day 4 the session starts with methods supported by TLM interface, implementing the TLM First In First Out (FIFO) and analyzing FIFO, TLM port & Export. Explains about UVM factory, UVM field macros and field arguments and explains the inbuilt logic of elements in testbench of UVM in EDA playground.

Day 5 the session starts with detailed explanation of elements of test bench of UVM like sequencer, driver, interface, monitor, agent, score board and environment. Discussion and Hands on session on System Verilog programs and assignments, Example work out on covered topic.

Day 6 the session starts UVM Phase, configuring through Configuration Database using SET and GET Method discussed about how to face the interview and had completed the session by conducting an exam.

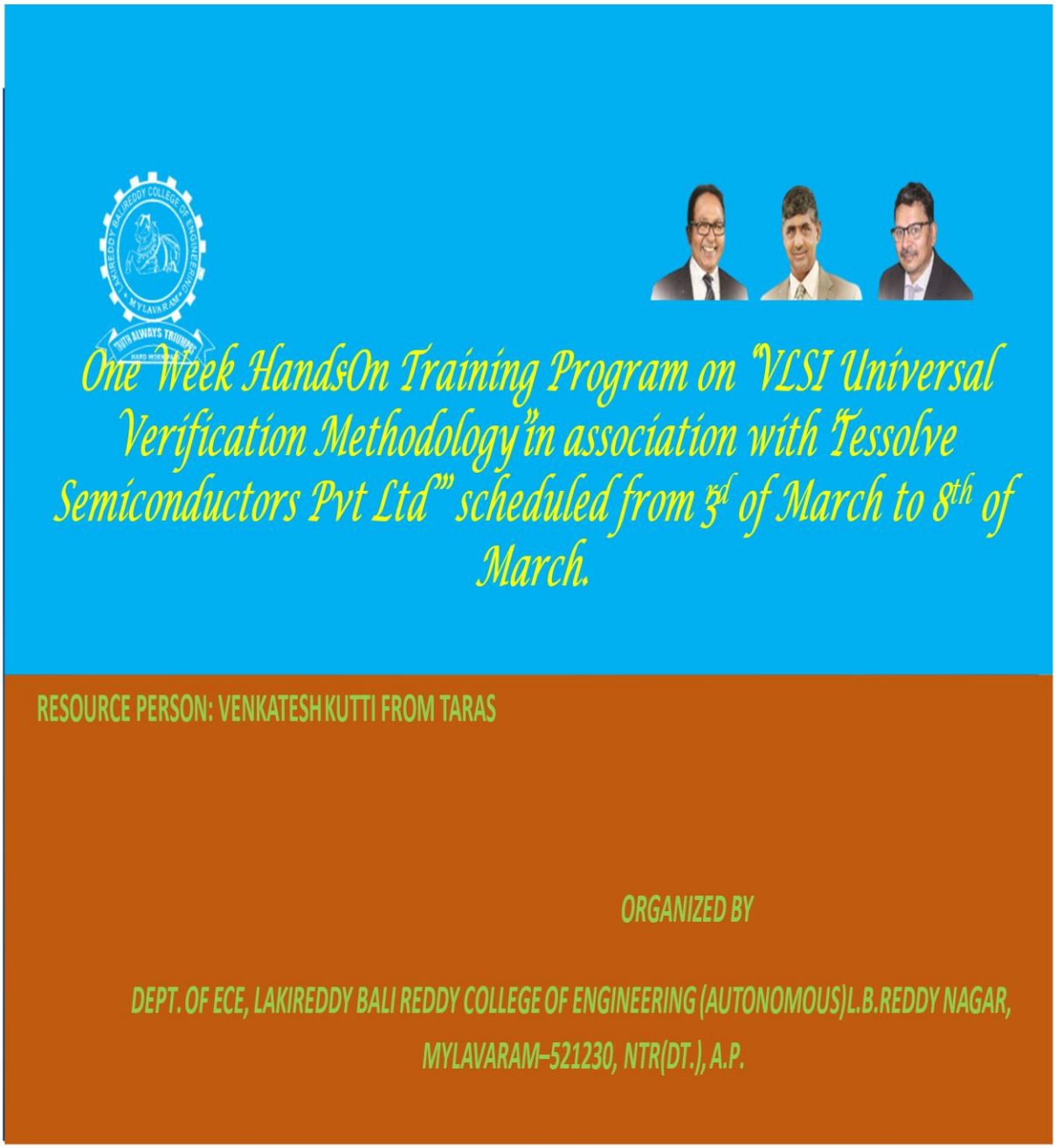
One Week Hands-On Training Program, Valedictory Session was held on 8th March 2025 at 3:40 pm by Coordinator Dr. B. Rambabu, Convener of program Dr. G. Srinivasulu and student Participants.

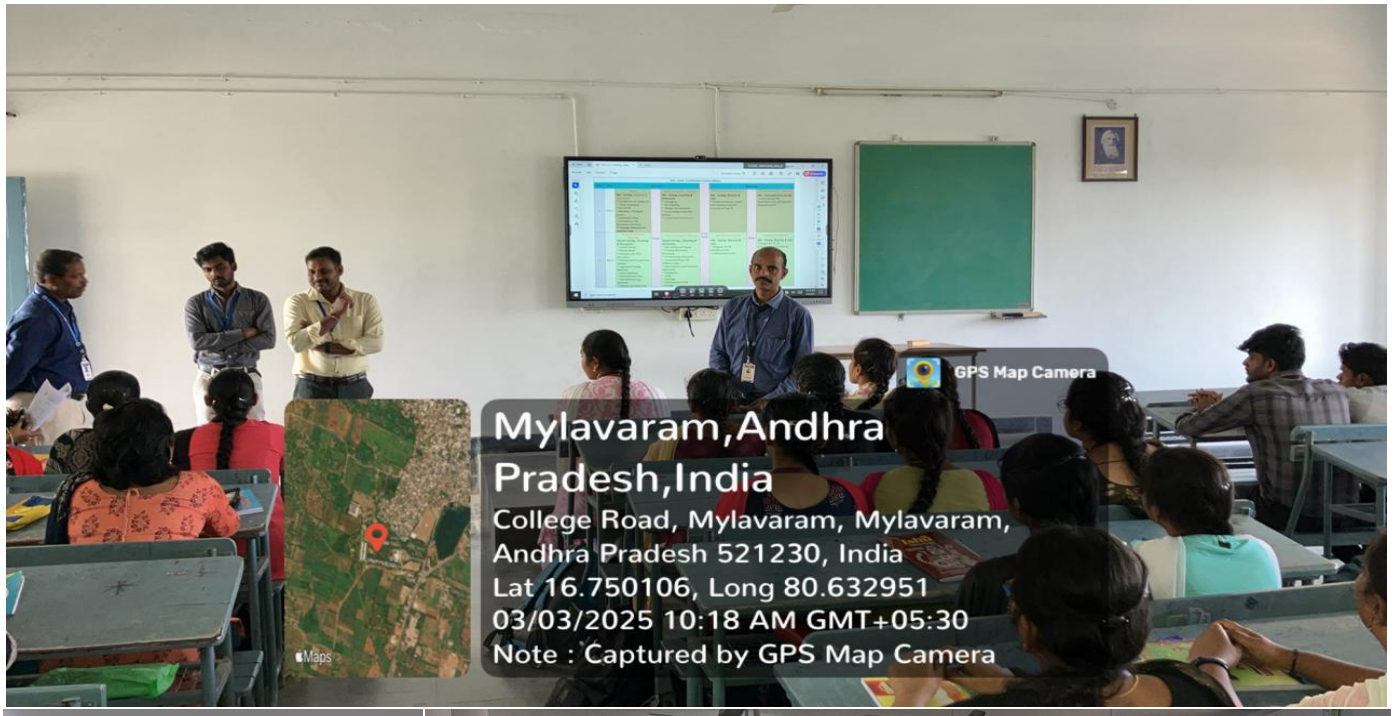
Dr. G. Srinivasulu in his valedictory addressing, conveyed his wishes to all the student participants. He motivated the students to keep learning new technologies coming in future for the career growth as well as organizational growth. Coordinator of the training program paid his gratitude to LBRCE Principal and Management for giving permission to conduct the program and the Resource person for their valuable time. Expressed the gratitude to the LBRCE management, Principal Dr. K. Appa Rao, for extending support and for providing an environment to complete training program successfully.

Feedback from the Participants:

The feedback of the students was very positive and motivational for the organizers. The students said that they gained knowledge on VLSI, understand the concepts of System Verilog and UVM with hands on experience. Students felt very happy for conducting the training program which is designed in view of industry requirements. All the students appreciated the sessions organized by the department of ECE and the arrangements made by the organizers. Certificates are issued to all the 68 participants from TARAS systems and Solutions.

Training Photo

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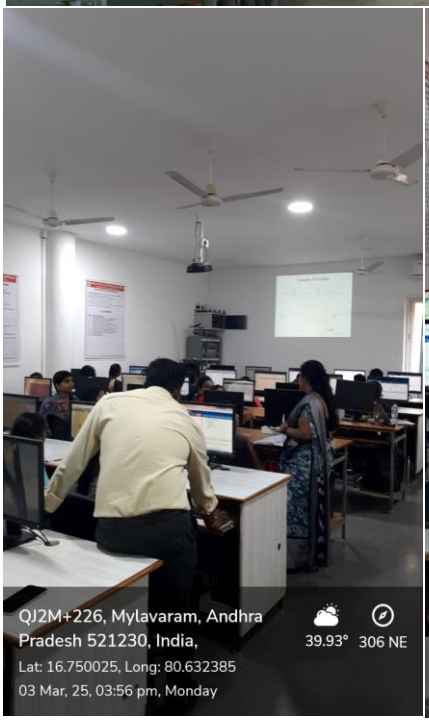
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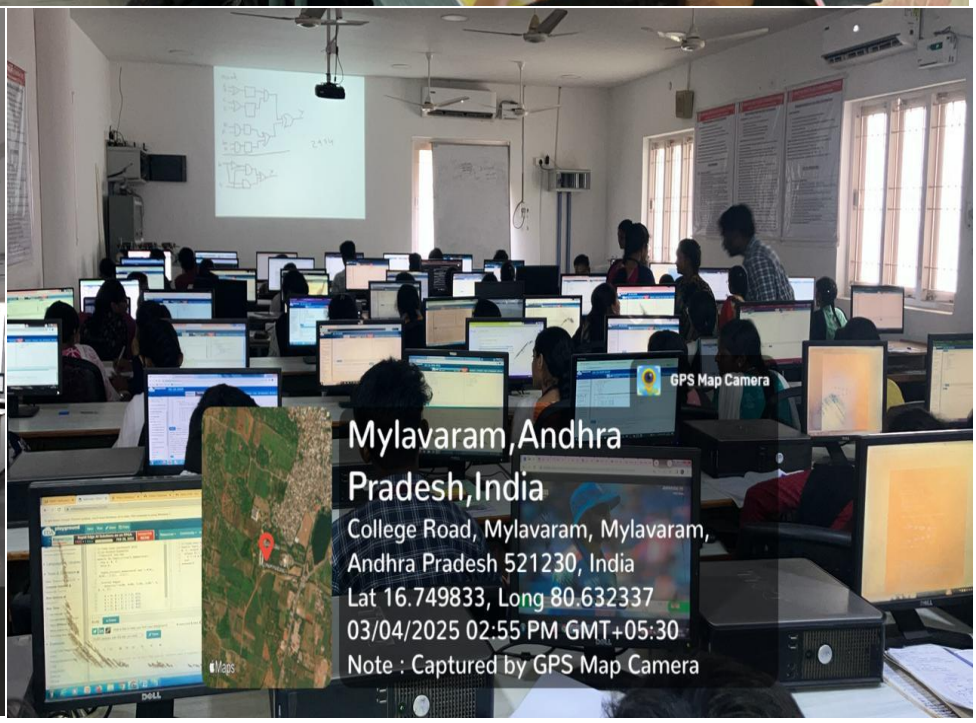
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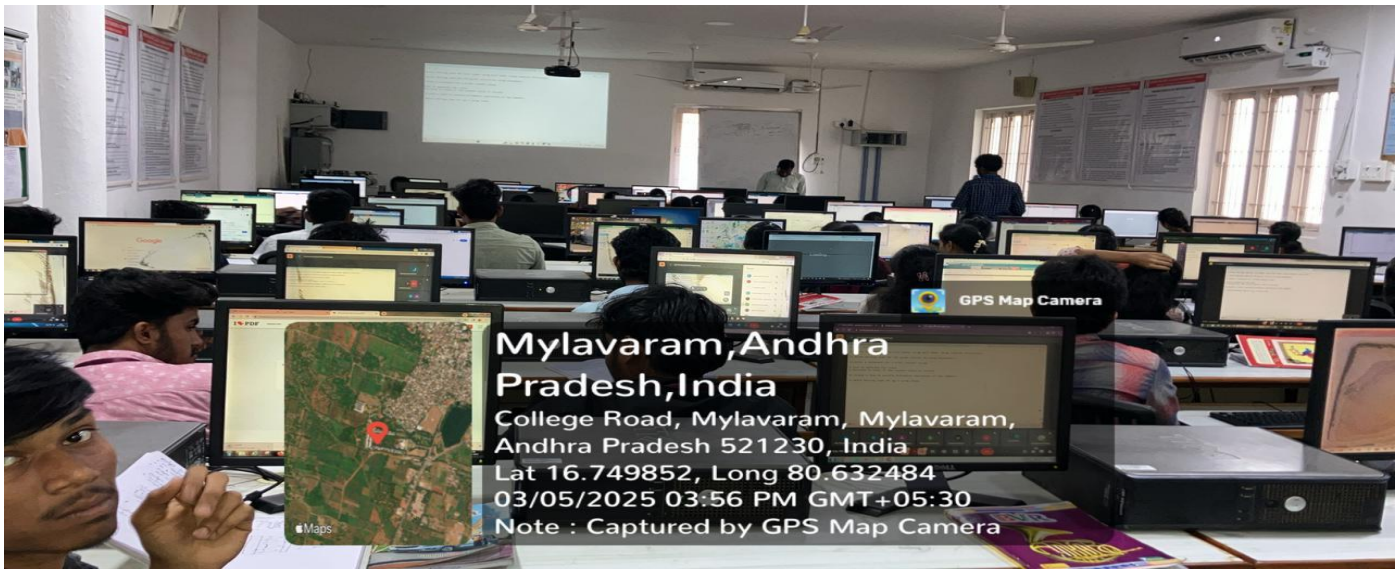
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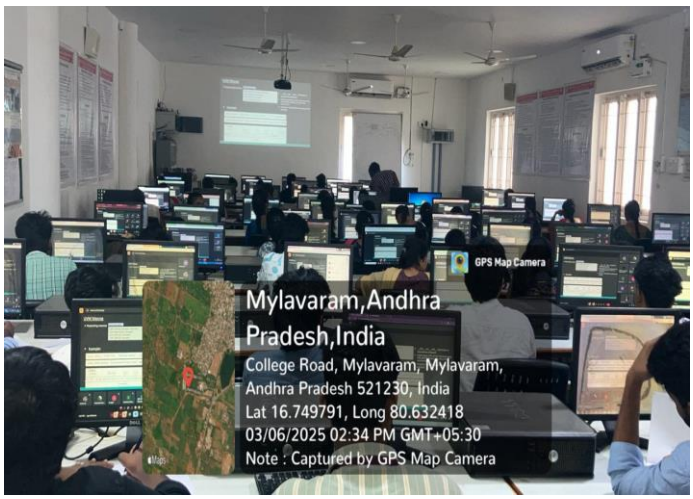

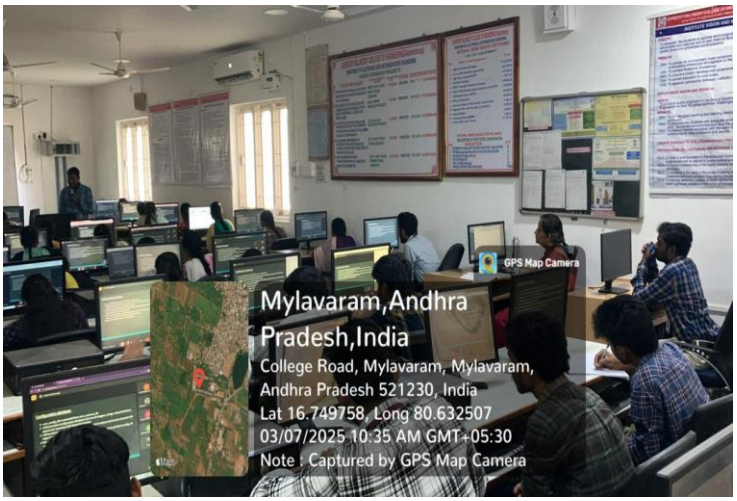

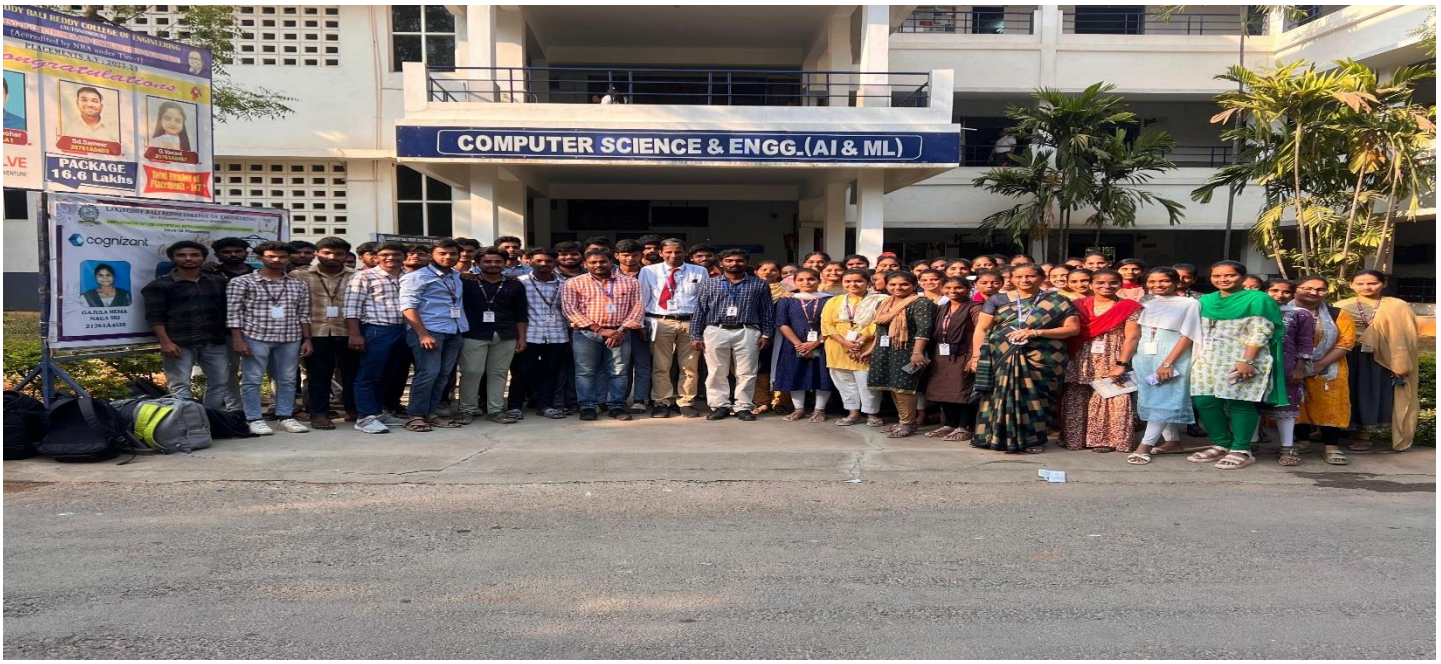

Co-Coordinator	Coordinator	Convener
T. Kalpana K. Bala Vani	B. Ram Babu	Dr. G. Srinivasulu