Unit-IV
Analog IC Building Blocks

VLSI DESIGN

MOS as Diode:

When the gate of the MOSFET is connected to the drain, it acts like a diode with characteristics similar to a pn-junction diode.

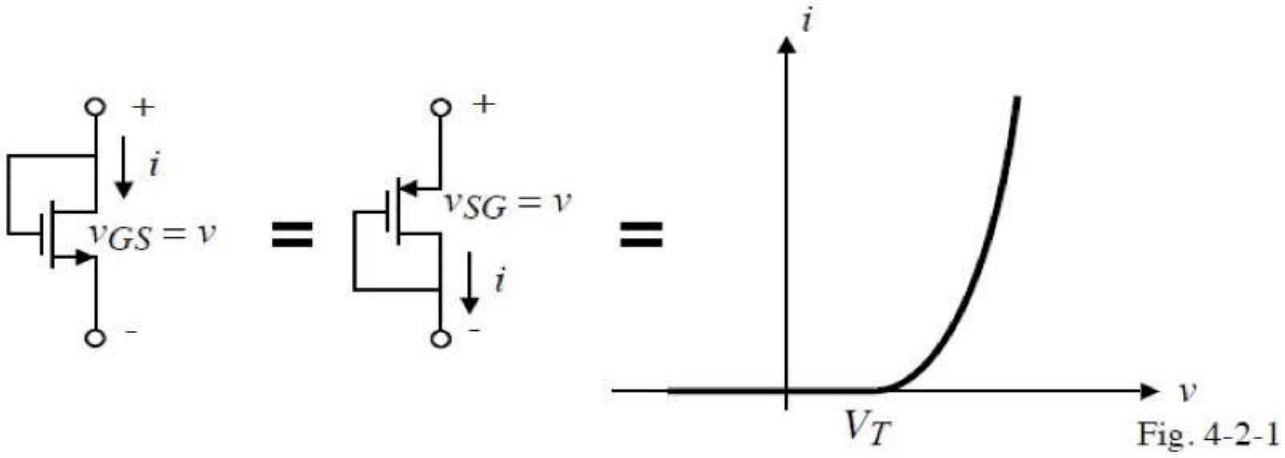


Fig. 4-2-1

Region of Operation

When the gate is connected to the drain of an enhancement MOSFET, the MOSFET is *always in the saturation region.*

$$v_{DS} \geq v_{GS} - V_T$$

$$\Rightarrow \quad v_D - v_S \geq v_G - v_S - V_T$$

$$\Rightarrow \quad v_D - v_G \geq -V_T$$

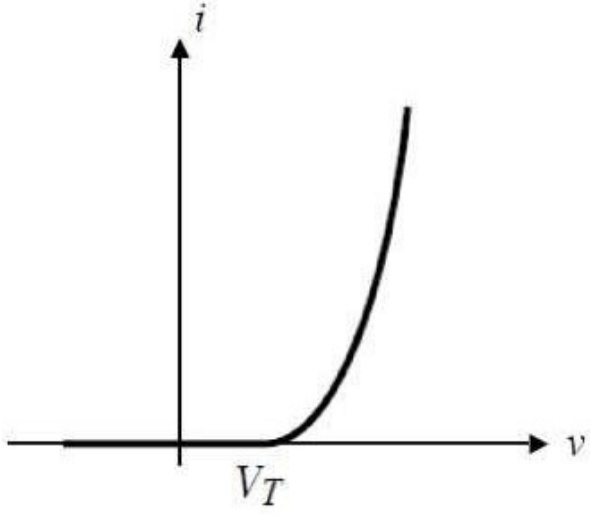
$$\Rightarrow \quad v_{DG} \geq -V_T$$

Since V_T *is always greater than zero for an enhancement device, then* $V_{DG} = 0$ *satisfies* the conditions for saturation.

Expression for Current/Voltage

$$I = I_D = \left(\frac{K'W}{2L}\right)[(V_{GS} - V_T)^2] = \frac{\beta}{2}(V_{GS} - V_T)^2$$

$$V = V_{GS} = V_{DS} = V_T + \sqrt{2I_D/\beta}$$

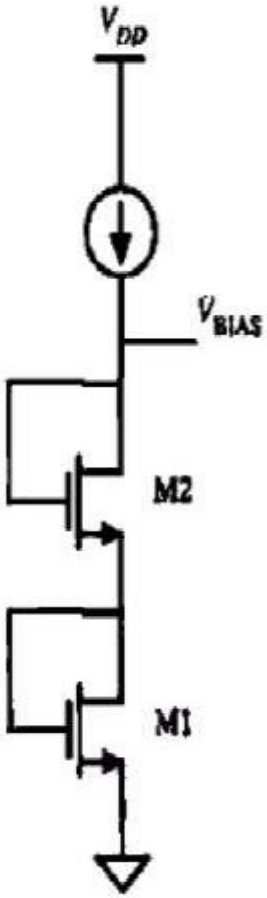


Applications of MOS diode

- The MOS diode is a component of Current Mirror circuits

- The MOS Diode is used for level translation

Application(To generate a Bias Voltage)

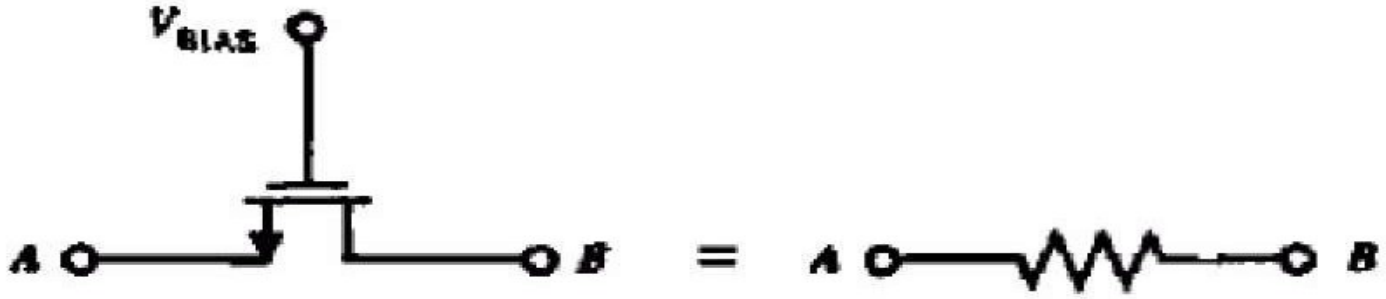


$$V_{DS} = \sqrt{2I/\beta} + V_T = V_{ON} + V_T$$

$$V_{BIAS} = V_{DS1} + V_{DS2} = 2V_{ON} + 2V_T$$

MOSFET as Active Resistor

The MOSFET Switch can be viewed as a resistor, where the transistor's Drain and Source form the two terminals of a floating resistor.



- MOSFET acts in non-saturation region. The Resistance can be given as:

$$r_{ds} = \frac{L}{K' W (V_{GS} - V_T)}$$

Current Source/Sinks

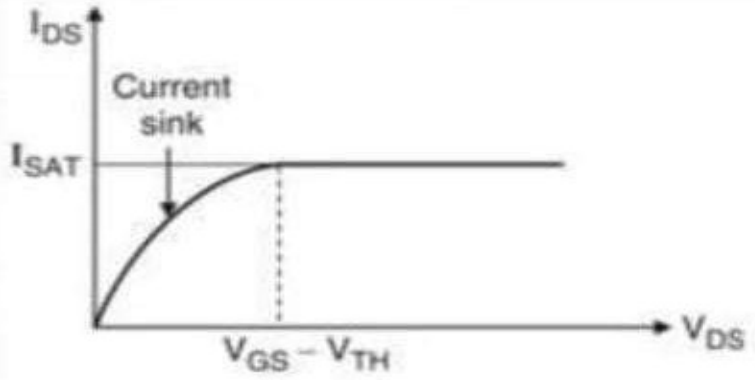
- **Source current** is the ability of the digital output/input port to supply **current**. **Sink current** is the ability of the port to receive **current**.

- These current sink and source are widely used for Biasing the MOS transistors for a particular functionality. It is therefore essential to learn about these components.

- The other components which are used for biasing are current mirrors and differential amplifiers.

Current Sink :

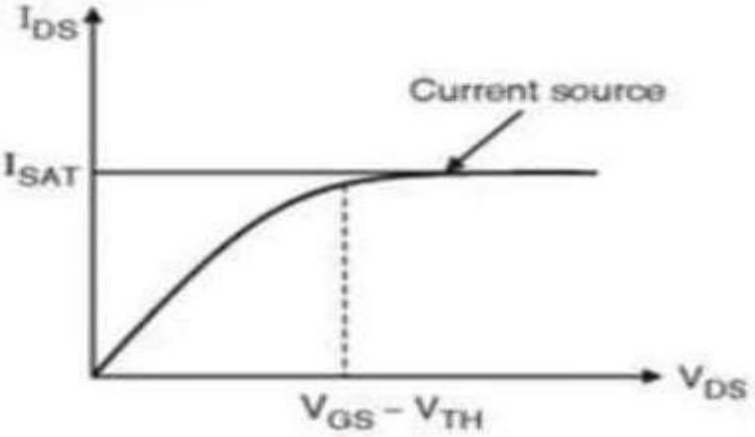
- Figure below shows the output characteristics of the NMOS transistor with showing the current sink region.
- From Figure, it can be seen that, if V_{DS} is less than the gate overdrive voltage then the transistor work as a current sink.



Output characteristics of NMOS transistor as current sink

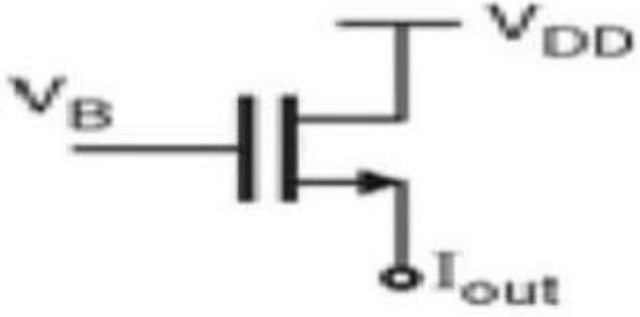
Current Sources

- In order to use the MOSFET as a current source, we will have to operate it in saturation region.
- If VDS is greater than the gate overdrive voltage then the drain current flowing through the device is constant. This current is called as Saturation current denoted by I_{SAT}.



Output characteristics of NMOS transistors as current source

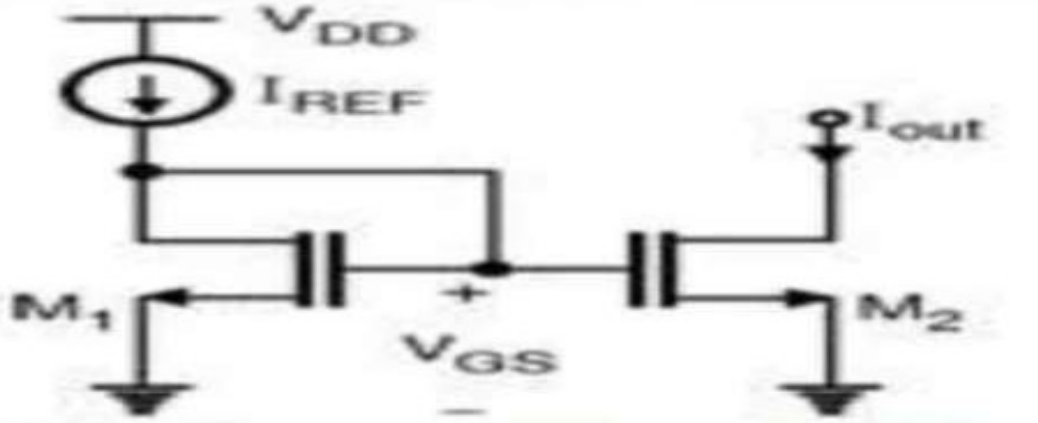
- Figure below shows the current source circuit based on NMOS transistor.
- The important application of current source is it can work as a load resistor in amplifier circuits with larger load resistance value.



NMOS current source

Current Mirrors :

- The current mirror circuits are based on the principle that, if the gate to source voltage of two identical MOSFETs are equal then the drain current flowing through them is equal.
- The basic current mirror circuit is shown in Figure below.



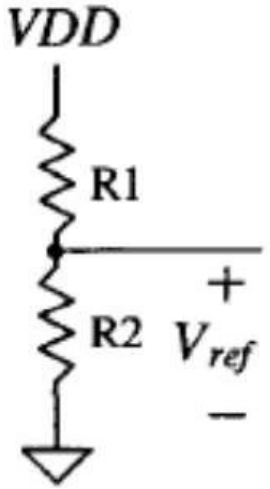
Basic current mirror

- By neglecting the channel length modulation of the two transistors the drain currents can be given as :
- $I_{REF} = m_n C_{ox} (V_{GS} - V_{TH})^2$
- and $I_{out} = m_n C_{ox} (V_{GS} - V_{TH})^2$
- If we take ratio of two equations, we get,
- = i.e. $I_{out} = I_{REF}$
- In basic current mirror circuit we have neglected the channel length modulation. In practice for short channel devices it results in significant error in mirroring the currents.

Voltage & Current References

- An Ideal reference should be independent of power supply, process and temperature variations.
- The term Reference is used when the current or voltage values have more precision and stability than ordinarily found in a source.
- A high performance voltage reference can be used to implement a high performance current reference and vice versa.
- Voltage and current references used to bias the current sources and sinks, differential amplifiers, operational amplifiers etc.....

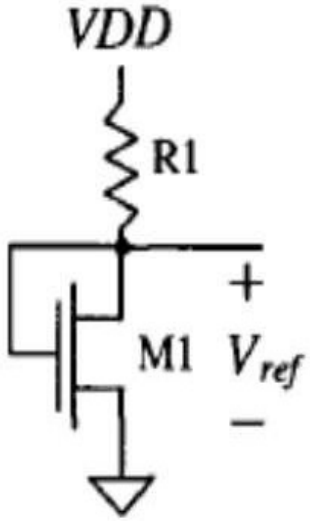
Implementation of voltage dividers in CMOS.



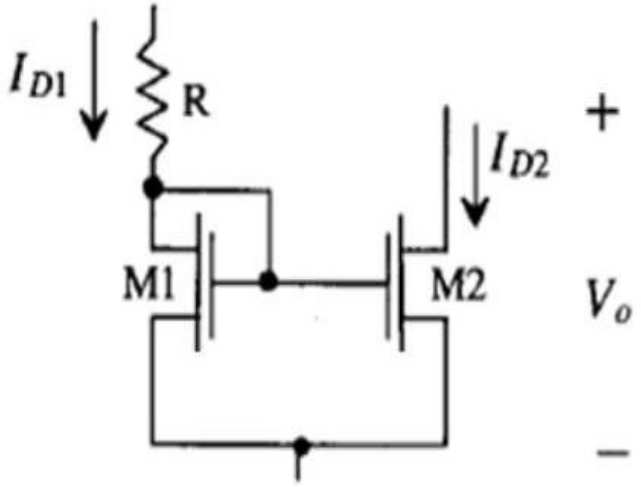
- To reduce power dissipation, the resistors must be made very large, which requires large area on die.

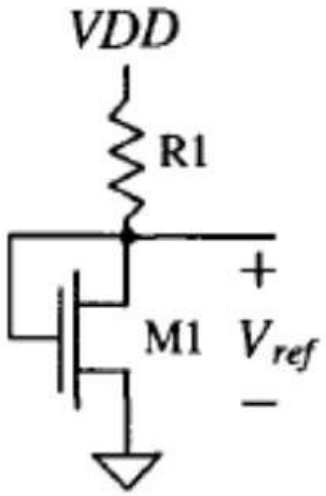
- Not practicable.

The Resistor - MOSFET Divider



- Used in simple current mirror to bias the M2 transistor





The reference voltage used in the resistor-MOSFET divider is equal to the V_{GS} of the MOSFET. $V_{ref} = V_{GS}$

Calculate V_{ref}?

$$I_D = \frac{VDD - V_{ref}}{R} = \frac{\beta_1}{2}(V_{ref} - V_{THN})^2$$

$$V_{ref} = V_{GS} = V_{THN} + \sqrt{\frac{2I_D}{\beta_1}} = V_{THN} + \sqrt{\frac{2(VDD - V_{ref})}{R \cdot \beta_1}}$$

Calculate Sensitivity of V_{ref} to V_{DD}?

The sensitivity of the reference voltage to *VDD*

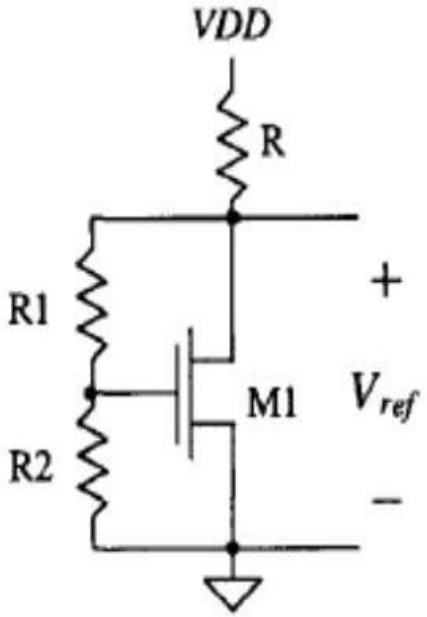
$$S_{VDD}^{V_{ref}} = \frac{VDD}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial VDD}$$

when $VDD >> V_{ref}$ is

$$V_{ref} = V_{THN} + \sqrt{\frac{2(VDD)}{R \cdot \beta_1}}$$

$$S_{VDD}^{V_{ref}} \approx \frac{1}{V_{THN} \cdot \sqrt{\frac{2R\beta_1}{VDD}} + 2}$$

How to achieve V_{ref} as more than V_{GS} ?

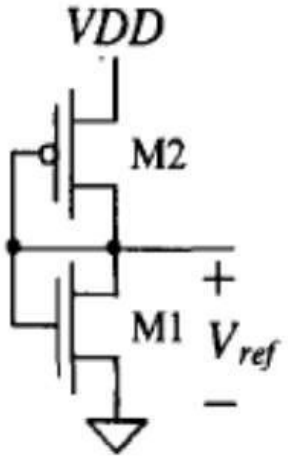


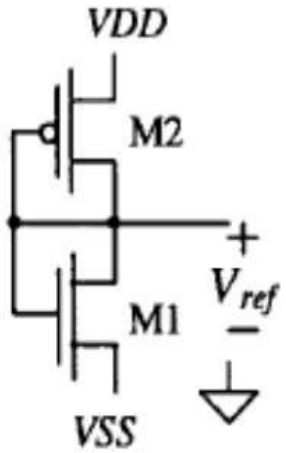
The reference voltage in this circuit is given by

$$V_{ref} = V_{GS}\left(\frac{R_1}{R_2} + 1\right)$$

Modification of the resistor-MOSFET voltage divider.

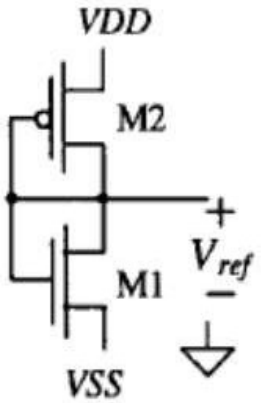
The MOSFET-Only Voltage Divider





Small layout because both are transistors

Calculate V_{ref} ?



Since $I_{D1} = I_{D2}$

$$\frac{\beta_1}{2}(V_{ref} - VSS - V_{THN})^2 = \frac{\beta_2}{2}(VDD - V_{ref} - V_{THP})^2$$

the reference voltage is

$$V_{ref} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}{\sqrt{\frac{\beta_1}{\beta_2}} + 1}$$

or

knowing the reference voltage and the power supply voltages gives

$$\frac{\beta_1}{\beta_2} = \left[\frac{VDD - V_{ref} - V_{THP}}{V_{ref} - VSS - V_{THN}}\right]^2$$

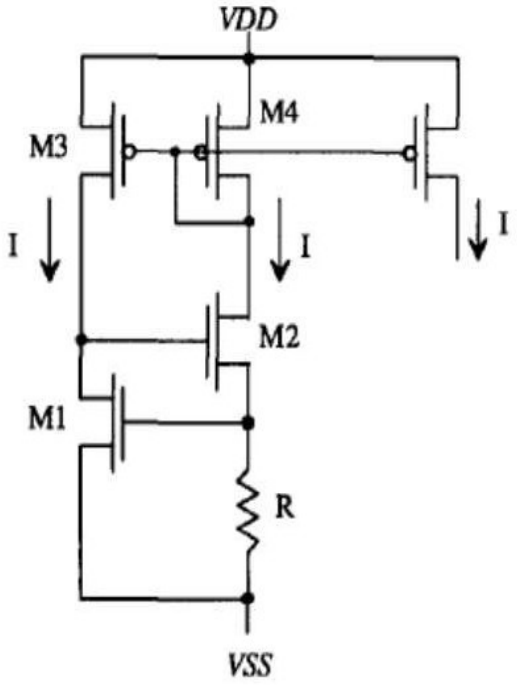
Current Source Self Biasing

Main drawback of References based on voltage divider are
very sensitive to supply voltage, process and temperature.

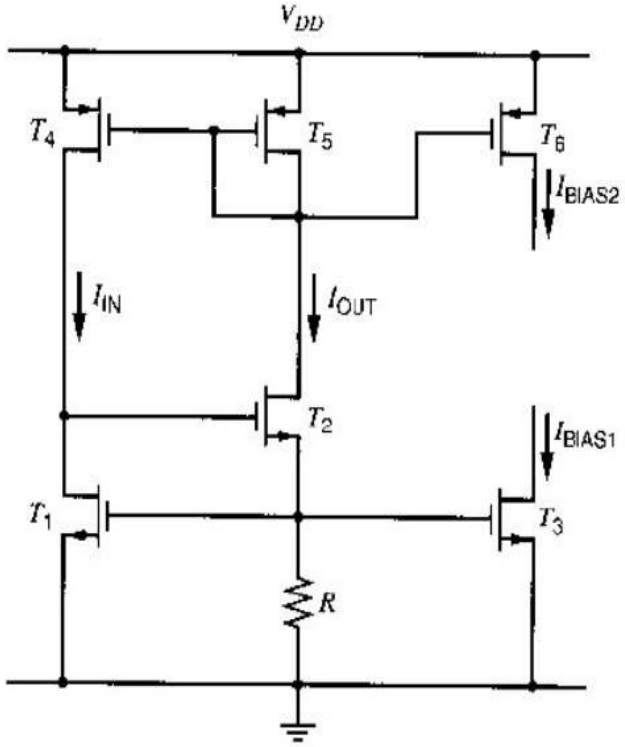
Three important types of current source self biasing are :

1. Threshold voltage referenced self biasing
2. Diode referenced self biasing
3. Thermal voltage referenced self biasing

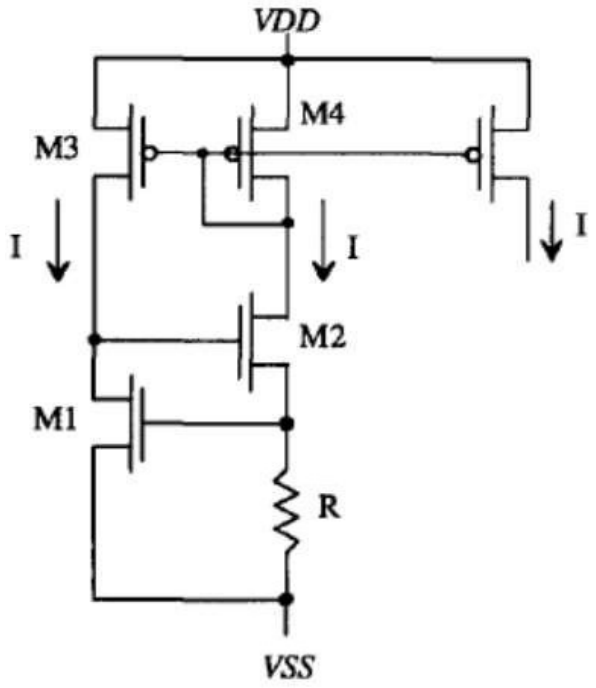
1. Threshold voltage referenced self biasing



Threshold reference self-biasing circuit.



Self-biasing V_t reference.



Threshold reference self-biasing circuit.

MOSFETs M3 and M4 force the same current to flow through M1 and M2. neglecting the output resistance of the MOSFETs and the body effect,

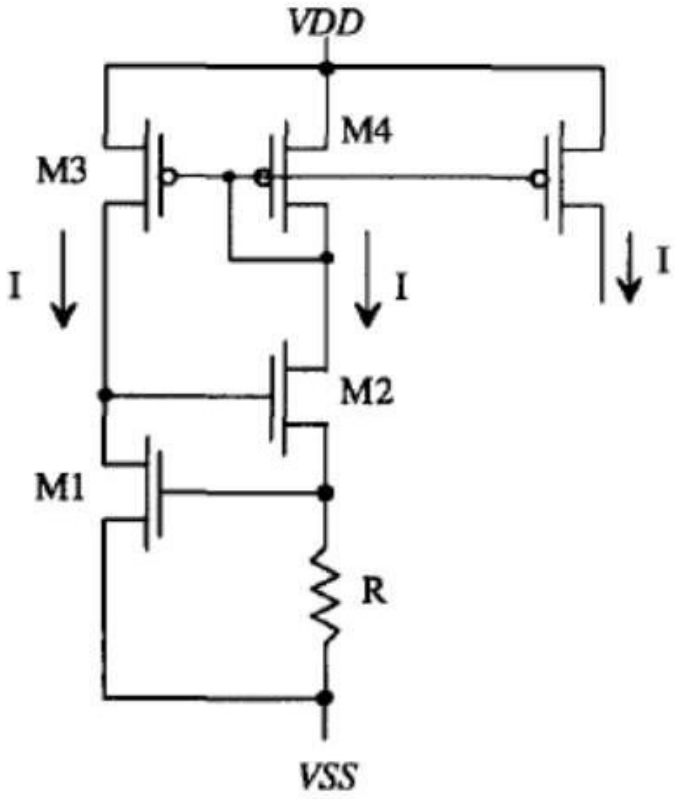
$$IR = V_{GS1} = V_{THN} + \sqrt{\frac{2I}{\beta_1}}$$

If β_1 is large, the current, I, is given by

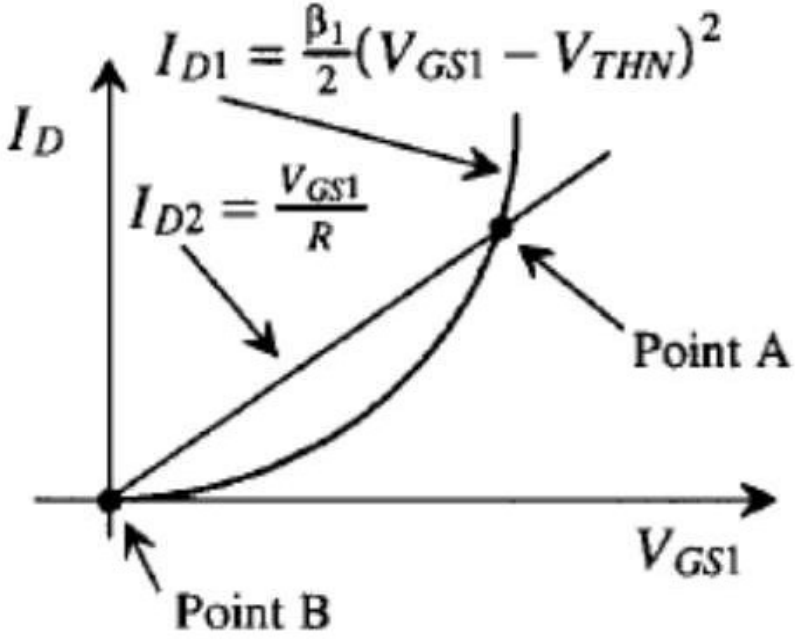
$$I \approx \frac{V_{THN}}{R}$$

Ideally the Reference current is independent of power supply.

Requirement of Start-Up circuit

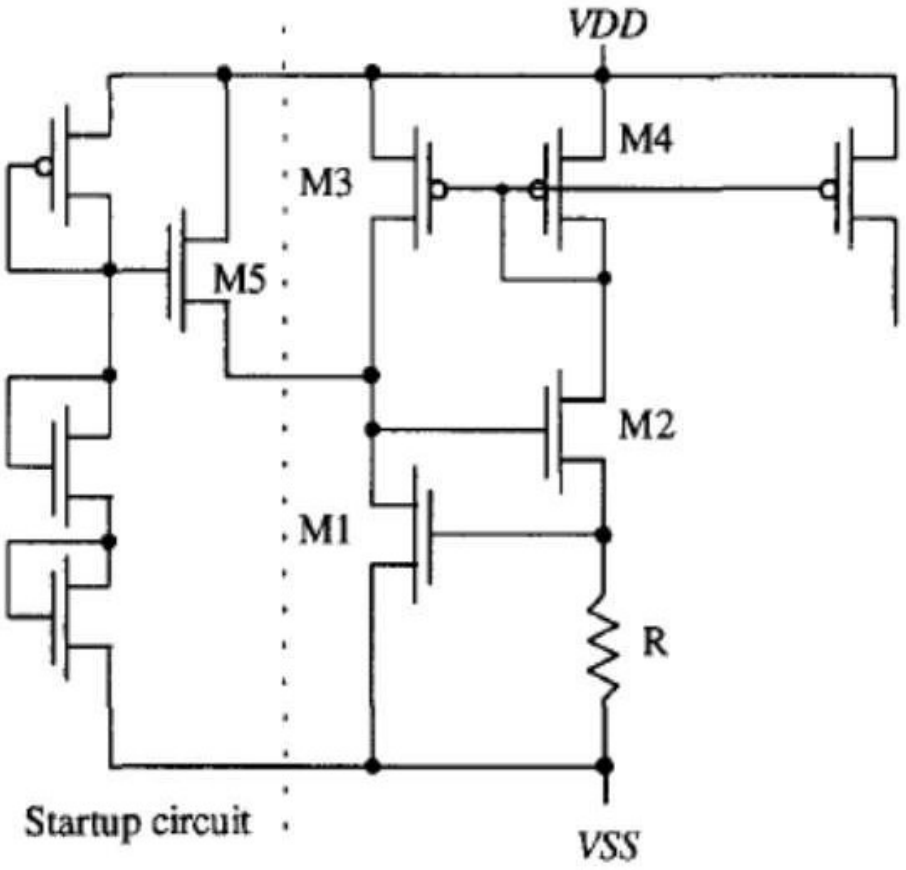


Threshold reference self-biasing circuit.



Two possible operating points of threshold bias circuit

Threshold Referenced Self biasing with start-up circuit



When $I_1 = I_2 = 0$ then
$V_{GS1} = I_2R = 0$ and $V_{DS1}=V_{GS2} = 0$.

Now M5 transistor provides current to flow through drain of M1. so I_1 increases and so I_2.

V_{G2} increases
V_{GS5} decreases
When I_1 reaches point A,
M5 turns off as $V_{GS5} < V_{t5}$.

The start up circuit will be idle until I_1 ($=I_2$) Becomes again zero.

Temperature Stable References

- The previous reference circuits failed to provide small values of temperature coefficient although sufficient power supply independence was achieved.
- This lecture introduces the bandgap voltage concept combined with power supply independence to create a very stable voltage reference in regard to both temperature and power supply variations.

Bandgap Voltage Reference Principle

The principle of the bandgap voltage reference is to balance the negative temperature coefficient of a pn junction with the positive temperature coefficient of the thermal voltage, $V_t = kT/q$.

Concept:

Result: References with TC_F's approaching 10 ppm/°C.

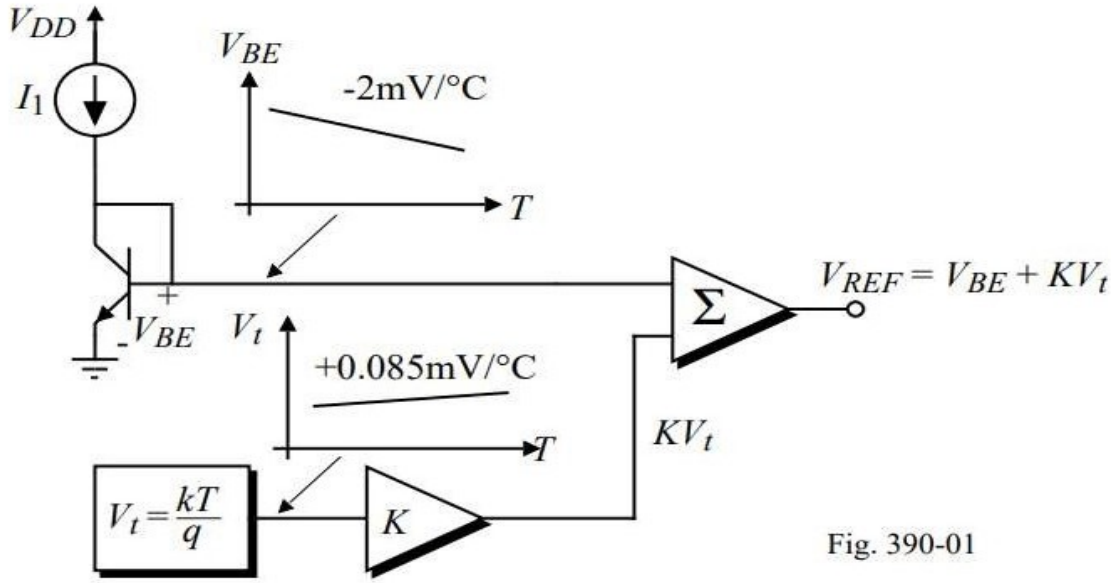


Fig. 390-01

Negative TC Voltage

The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a *pn*-junction diode exhibits a negative TC. We first obtain the expression for the TC in terms of readily-available quantities.

$$I_C = I_S \exp(V_{BE}/V_T)$$

I_S is proportional to $\mu k T n_i^2$

$$n_i^2 \propto T^3 \exp[-E_g/(kT)]$$

$$I_S = bT^{4+m} \exp \frac{-E_g}{kT}$$

$$V_{BE} = V_T \ln(I_C/I_S)$$

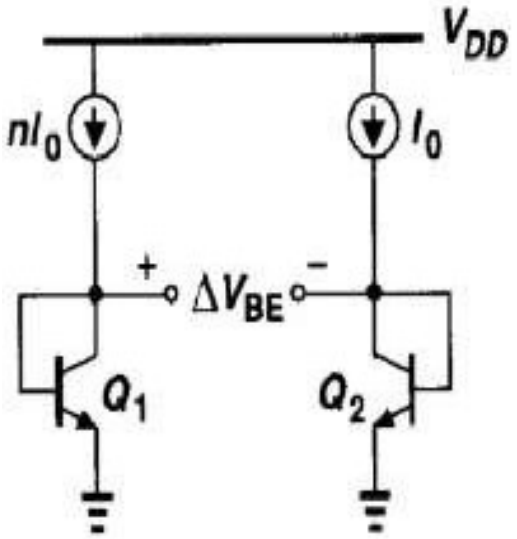
$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}.$$

With $V_{BE} \approx 750\,\text{mV}$ and $T = 300^\circ\text{K}$, $\partial V_{BE}/\partial T \approx -1.5\,\text{mV}/^\circ\text{K}$

Positive TC Voltage

- It was recognised in 1964 that if two bipolar transistors operate at unequal current densities then the difference between their base-emitter voltages is proportional to the absolute temperature

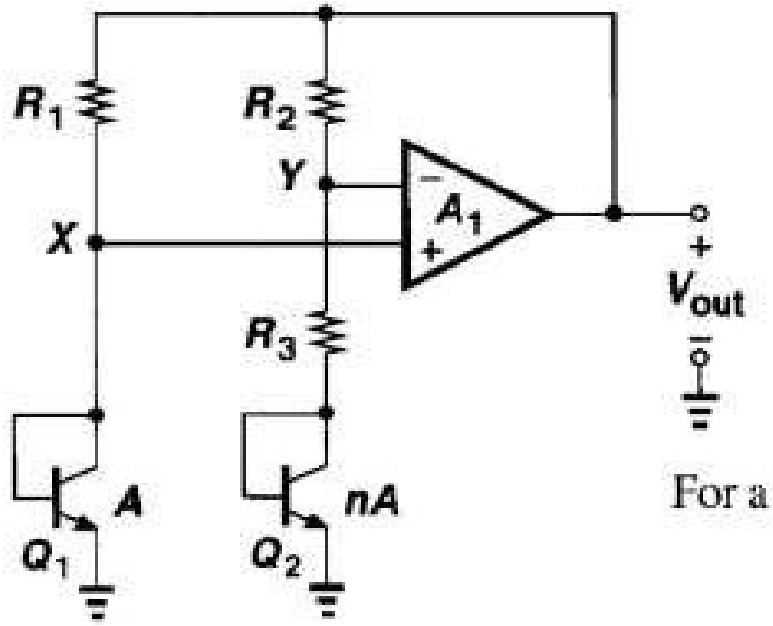


$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} \\ &= V_T \ln n.\end{aligned}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n.$$

With the negative- and positive-TC voltages obtained above, we can now develop a reference having a nominally zero temperature coefficient. We write $V_{REF} = \alpha_1 V_{BE} + \alpha_2(V_T \ln n)$, where $V_T \ln n$ is the difference between the base-emitter voltages of the two bipolar transistors operating at different current densities. How do we choose α_1 and α_2? Since at room temperature $\partial V_{BE}/\partial T \approx -1.5$ mV/°K whereas $\partial V_T/\partial T \approx +0.087$ mV/°K, we may set $\alpha_1 = 1$ and choose $\alpha_2 \ln n$ such that $(\alpha_2 \ln n)(0.087 \text{ mV/°K}) = 1.5$ mV/°K. That is, $\alpha_2 \ln n \approx 17.2$, indicating that for zero TC:

$$\begin{aligned} V_{REF} &\approx V_{BE} + 17.2 V_T \\ &\approx 1.25 \text{ V}. \end{aligned}$$



$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2)$$

$$= V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right)$$

For a zero TC, we must have $(1 + R_2/R_3) \ln n \approx 17.2$

Op-amps Introduction

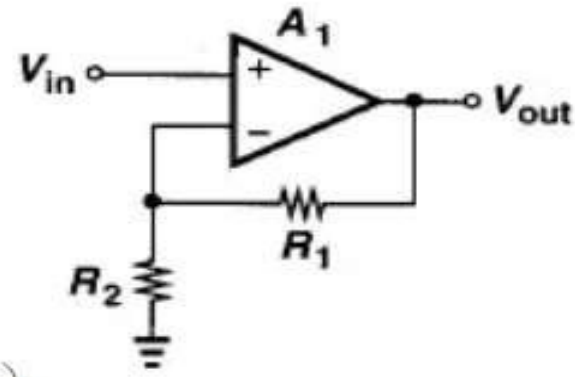
- Operational amplifiers (op amps) are an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering.

Performance parameters

1. Gain

   - Example: the circuit is designed for a nominal of 10, i.e., $1 + R_1/R_2 = 10$.

     The close-loop gain:



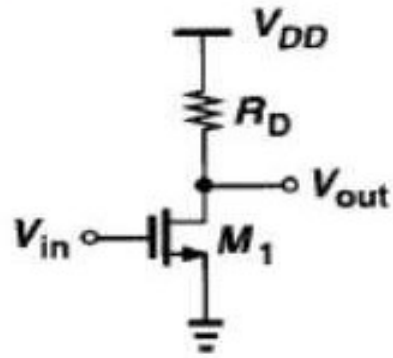
$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1} = \frac{R_1 + R_2}{R_2} \cdot \frac{A_1}{\frac{R_1 + R_2}{R_2} + A_1}$$

If $A_1 >> (R_1 + R_2)/R_2$, then $\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right)\left(1 - \frac{R_1 + R_2}{R_2}\frac{1}{A_1}\right)$

The term $(R_1 + R_2)/(R_2 A_1) = (1 + R_1/R_2)/ A_1$ represents the relative error.
To achieve a gain error less than 1%, we must have $A_1 > 1000$.

   - Discussion

     Simple CS stage – an open-loop implementation:



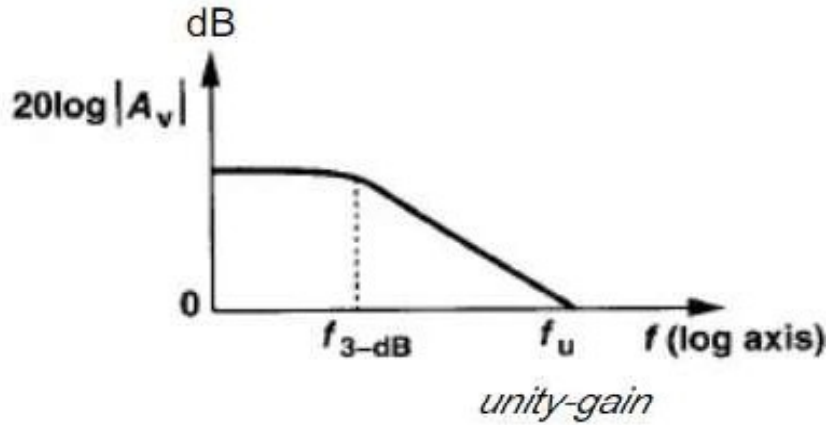
$$\left|\frac{V_{out}}{V_{in}}\right| = g_m R_D = 10$$

However, it is difficult to guarantee an error less than 1%.
The variations in the mobility and gate oxide thickness of the transistor and the value of the resistor typically yield an error greater than 20%.

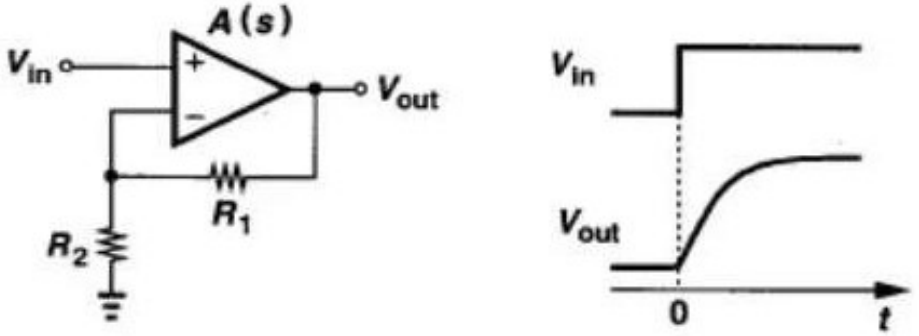
Performance parameters (cont'd)

❷ Small-signal bandwidth

Gain roll-off with frequency



❸ Large-signal bandwidth – slew rate



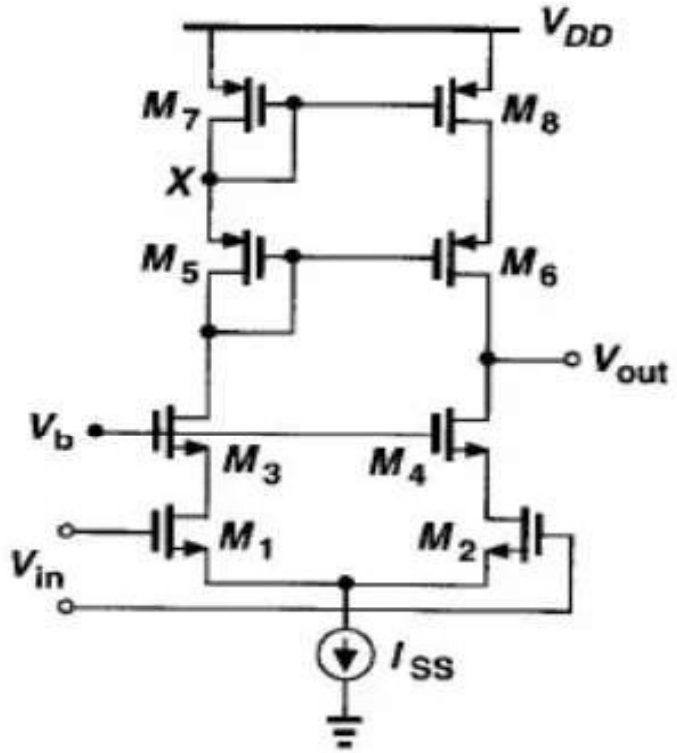
Performance parameters (cont'd)

❹ Output swing – Most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitudes.

❺ Linearity – Open-loop op amps suffer from substantial nonlinearity. For example, the input pair $M_1 - M_2$ exhibits a nonilinear relationship between its differential drain current and input voltage. In many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain.

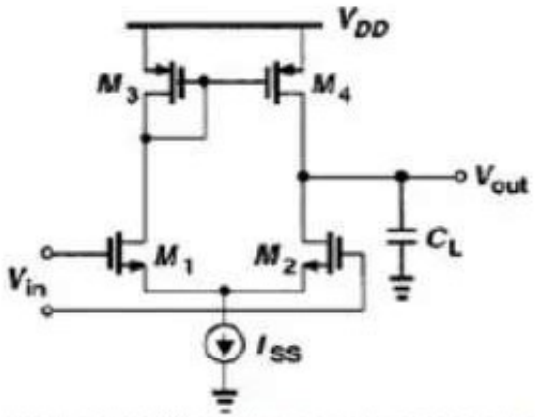
❻ Noise and offset – The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality.

❼ Supply rejection – Op amps are often employed in mixed-signal systems and sometimes connected to noise digital supply lines. Thus, the performance of op amps in the presence of supply noise is quite important. For this reason, fully differential topologies are preferred.

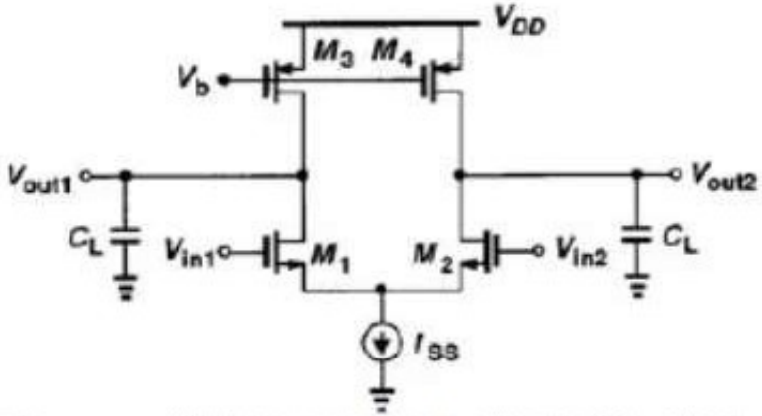


One-stage op amps

Simple op amp topologies



Differential input & *single-ended* output



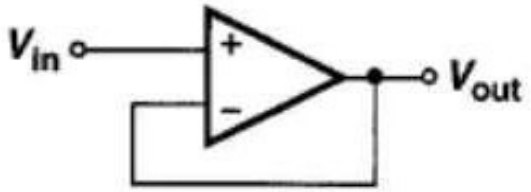
Differential input & *differential* output

For small-signal:

- Low frequency gain = $g_{mN}(r_{oN} \| r_{oP})$. In general, this value hardly exceeds 20 in submicron devices with typical current levels.
- The bandwidth is usually determined by the load capacitance, C_L.
- The circuits suffer from noise contributions of M_1-M_4. In all op amp topologies, at least four devices contribute to the input noise: two input transistors and two "load" transistors.

Unit-gain buffer

Input common-mode voltage range

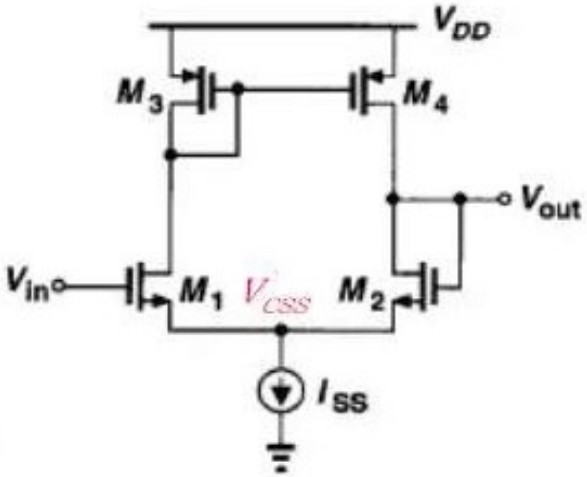


$$V_{in,min} = V_{CSS} + V_{GS1}$$
$$V_{in,max} = V_{DD} - |V_{GS3}| + V_{TH1}$$

If each device has a threshold voltage of 0.7V and an overdrive of 0.3V, then $V_{in,min}$ = 1.3V, and $V_{in,max}$ = 2.7V. Thus, the input CM range equals 1.4V with a 3-V supply.

Output impedance

$$R_{out} = \frac{R_{out,open}}{1 + \beta A_{v,open}} = \frac{r_{oP} \| r_{oN}}{1 + g_{mN}(r_{oP} \| r_{oN})} \approx \frac{1}{g_{mN}}$$

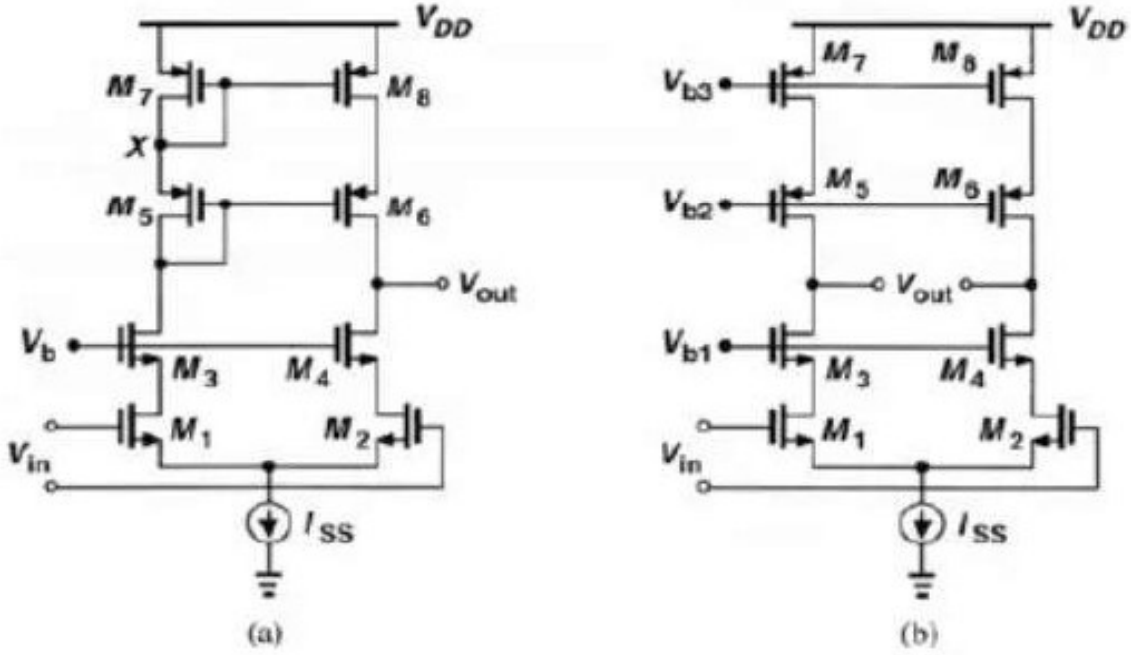


The close-loop output impedance is relatively *independent* of the open-loop output impedance. Allowing us to design high-gain op amps by *increasing* the open-loop output impedance while still achieving a relatively low close-loop output impedance.

Telescope cascode op amps

In order to achieve a high gain, the differential cascode topologies can be used.

Low-frequency gain $A_v = g_{mN}[(g_{mN} r_{oN}^2) \parallel (g_{mP} r_{oP}^2)]$, but at the cost of output swing and adding poles.



Telescope cascode op amps (cont'd)

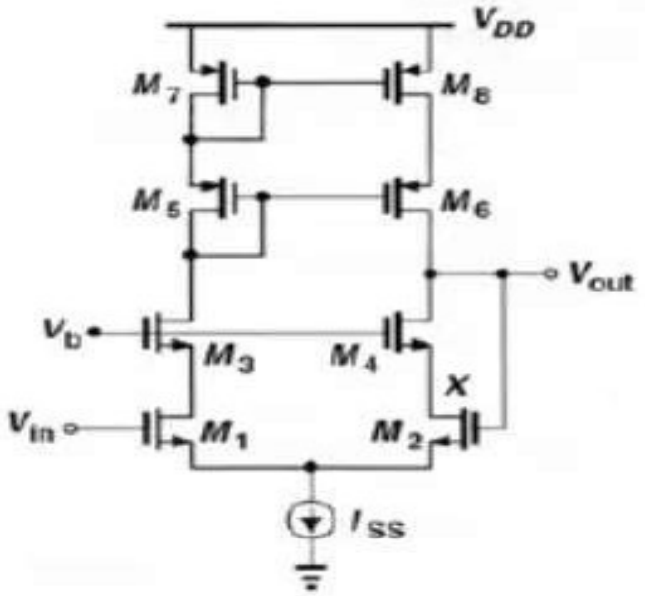
Cascode op amp with input and output shorted – unit gain feedback topology

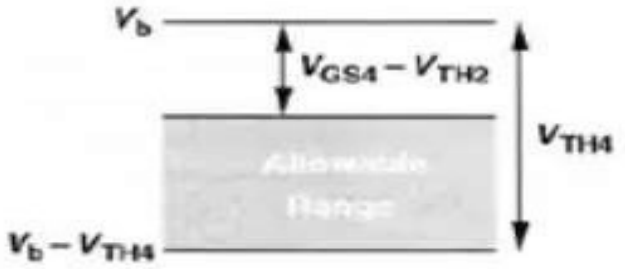
- Output swing: $M2$ and $M4$ in saturation:

$$\begin{cases} V_{out} \le V_X + V_{TH2} \\ V_{out} \ge V_b - V_{TH4} \end{cases} \Rightarrow V_b - V_{TH4} \le V_{out} \le V_b - V_{GS4} + V_{TH2}$$

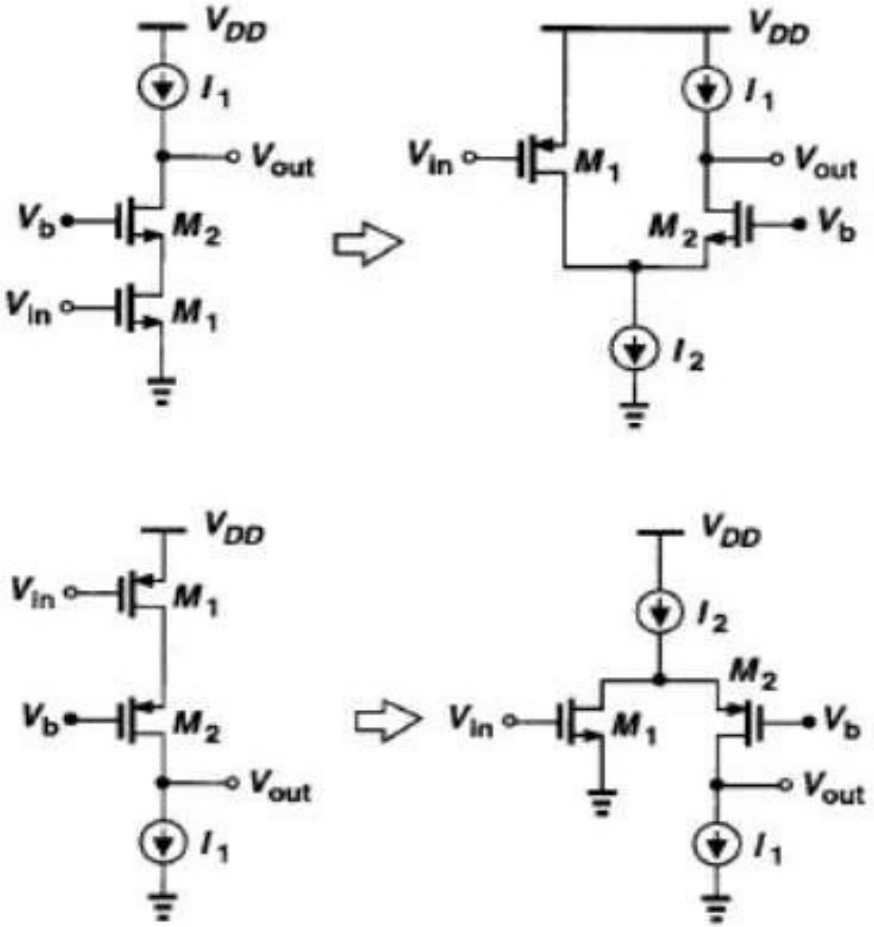
the voltage range $V_{max} - V_{min} = V_{TH4} - (V_{GS4} - V_{TH2})$

- Since the op amp attempts to force V_{out} to be equal to V_{in}, for $V_{in} < V_b - V_{TH4}$, we have $V_{out} \approx V_{in}$ and M_4 is in triode region while others are saturated. Under this condition, the open-loop gain of the op amp is reduced.
- As V_{in} and V_{out} hence exceed $V_b - V_{TH4}$, M_4 enters saturation and the open-loop gain reaches a maximum. For $V_b - V_{TH4} < V_{in} < V_b - (V_{GS4} - V_{TH2})$, both M_2 and M_4 are saturated and for $V_{in} > V_b - (V_{GS4} - V_{TH2})$, M_2 and M_1 enter the triode region, degrading the gain. Thus, a cascode op amp is rarely used as a unit-gain buffer.



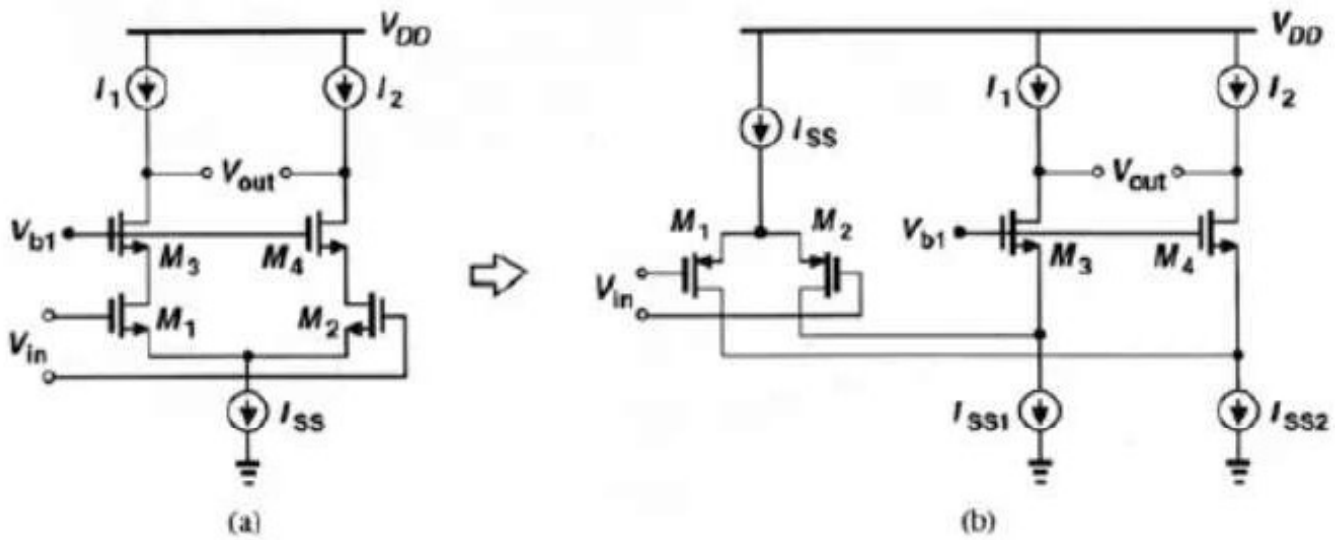


Folded cascode op amps



In order to alleviate the drawbacks of telescopic cascode op amps. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not *stack* the cascode transistor on the top of the input device.

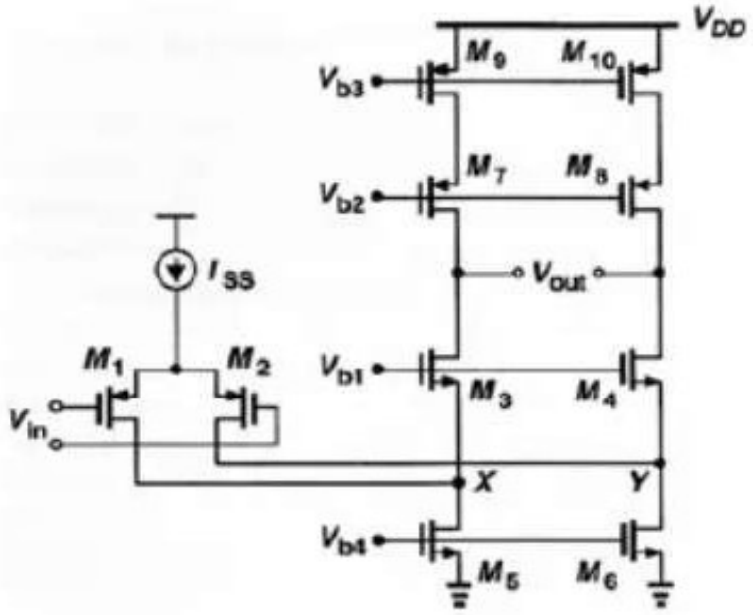
Folded cascode op amps (cont'd)



- Two important differences between the two circuits:
  - In Fig.(a), one bias current, I_{SS}, provides the drain current of both the input transistors and the cascode devices.
    In Fig.(b), the input pair requires an additional bias current, $I_{SS1} = I_{SS}/2 + I_{D3}$.
  - In Fig.(a), the input CM level cannot exceed $V_{b1} - V_{GS3} + V_{TH1}$,whereas in Fig.(b), it cannot be *less* than $V_{b1} - V_{GS3} + |V_{TH1}|$.
- In Fig.(b), it is possible to tie the *n*-well of M_1 and M_2 to their common source point.

Folded cascode op amps (cont'd)

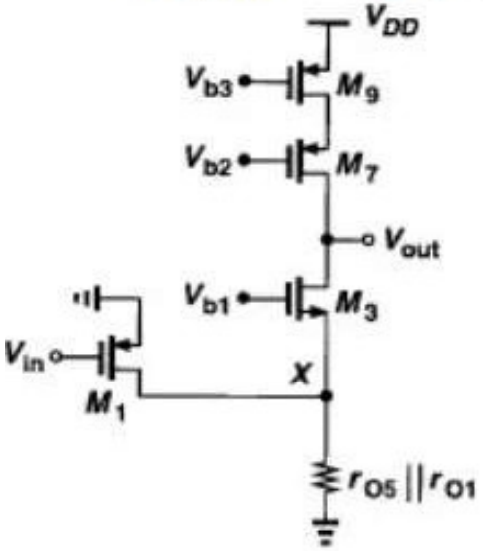
Folded cascode op amp with cascode PMOS loads



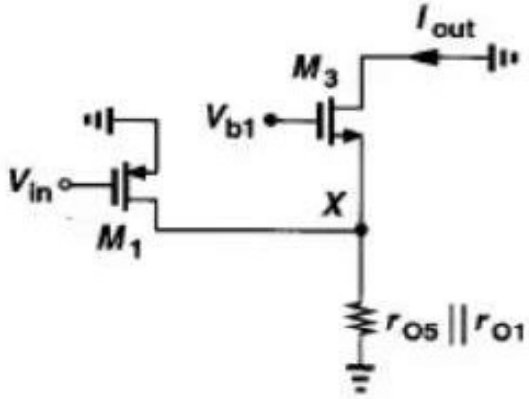
- Max. output voltage swing: With proper choice of V_{b1} and V_{b2},
  Peak-peak swing = $[V_{DD} - (|V_{OD7}| + |V_{OD9}|)] - (V_{OD3} + V_{OD5})$ for one side.
- The swing is lager by the overdrive of the tail current source in the telescopic cascode. M_5 and M_6 may require a high overdrive voltage if their capacitance contribution to nodes X and Y is to be minimized.

Folded cascode op amps (cont'd)

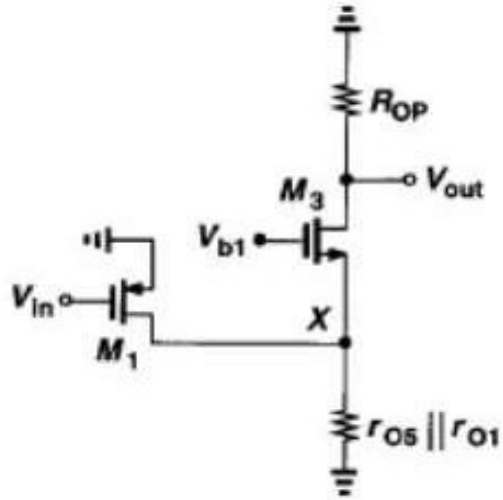
Small-signal voltage gain



Half circuit



Equivalent circuit with output shorted to ground



Equivalent circuit with output open

$$|A_v| = G_m R_{out}$$

Since $(g_{m3}+g_{mb3})^{-1} || r_{o3} << r_{o1} || r_{o5}$,

$I_{out} \approx I_{D1}$. That is $G_m \approx g_{m1}$.

$$R_{OP} \approx (g_{m7} + g_{mb7})\, r_{o7}\, r_{o9}$$

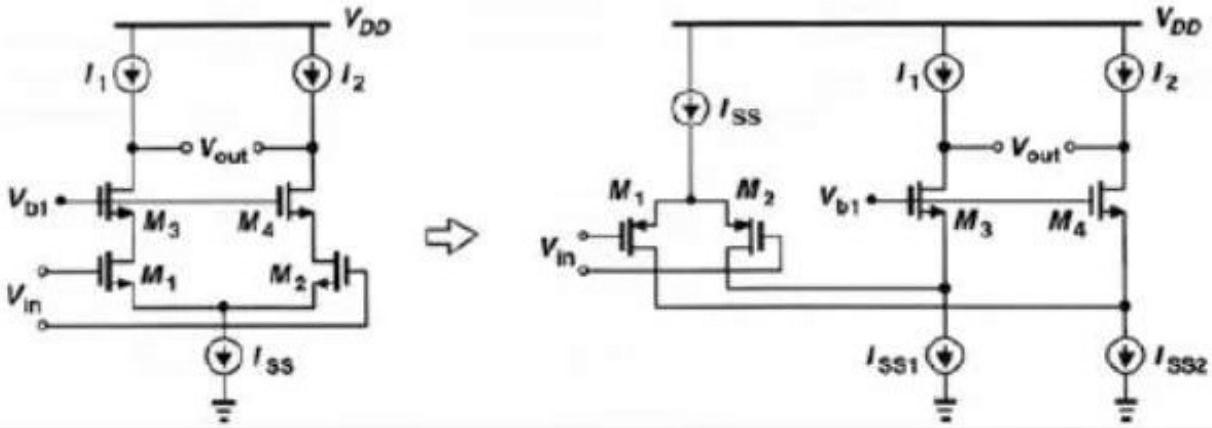
$$R_{out} \approx R_{OP} || \, [(g_{m3}+g_{mb3}) r_{o3} (r_{o1} || r_{o5})]$$

Thus, $|A_v| \approx g_{m1} \{[(g_{m3}+g_{mb3}) r_{o3} (r_{o1} || r_{o5})] \, || \, [(g_{m7} + g_{mb7})\, r_{o7}\, r_{o9}]\}$

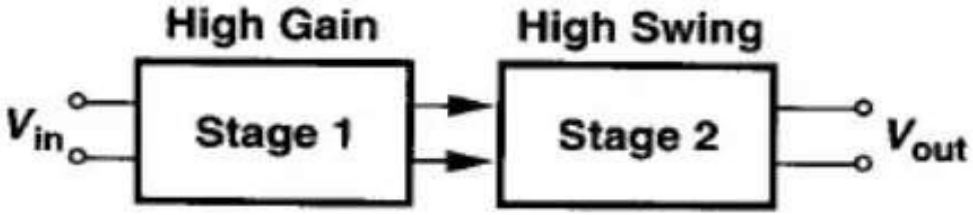
The gain is usually two or three times lower than of a comparable telescopic cascode.

Telescopic- & folded-cascode op amps: Discussion

- The overall voltage swing of a folded-cascode op amp is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies, and higher noise.
- Folded-cascode op amps are used quite widely, even more than telescopic topologies, because the input and outputs can be shorted together and the choice of the input common-mode level is easier.
  - In a telescopic op amp, *three* voltages must be defined carefully: the input CM level and the gate bias voltages of the PMOS and NMOS cascode transistors, whereas in folded-cascode configurations only the latter two are critical.
  - In folded-cascode op amps, the capability of handling input CM levels are close to one of the supply rails.

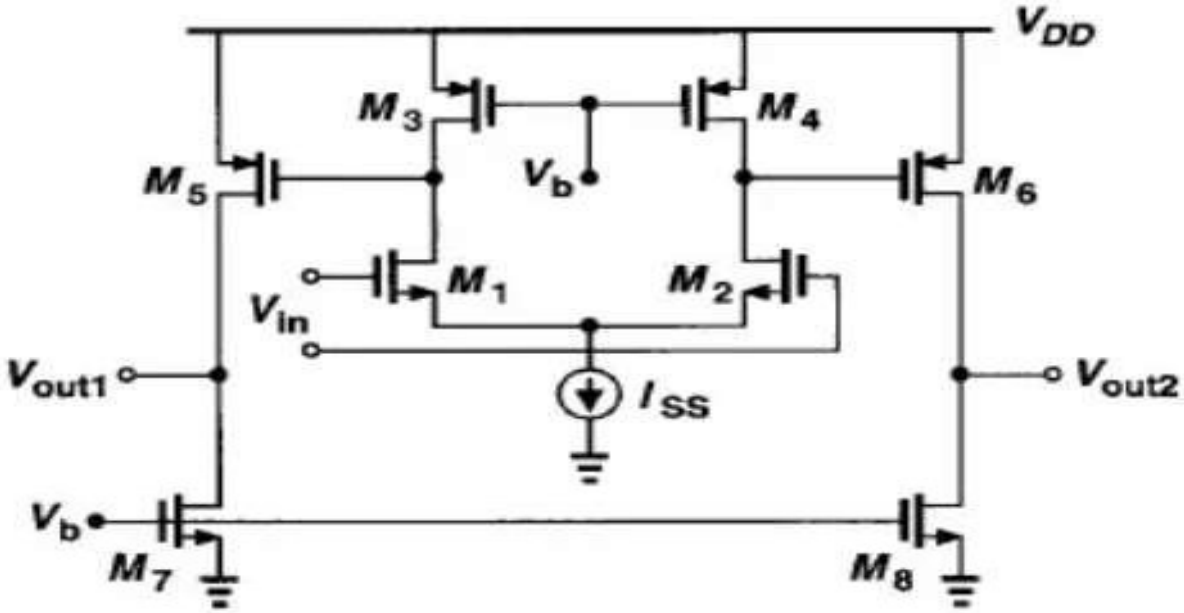


Two-stage op amps



- The gain of one-stage topologies is limited to the input pair transconductance and the output impedance.
- Two-stage op amps consist of first stage providing a high gain and the second providing large swing. The first stage incorporates various amplifier topologies, but the second stage is typically configured as a simple common- source stage to allow maximum output swings.
- Can we cascade more than two stages to achieve a higher gain?
  Each gain stage introduces at least one pole in the open-loop transfer function, making it difficult to guarantee stability in a feedback system using such an op amp. For this reason, op amps having more than two stages are rarely used.

Simple implementation of a two-stage op amp



Gain:

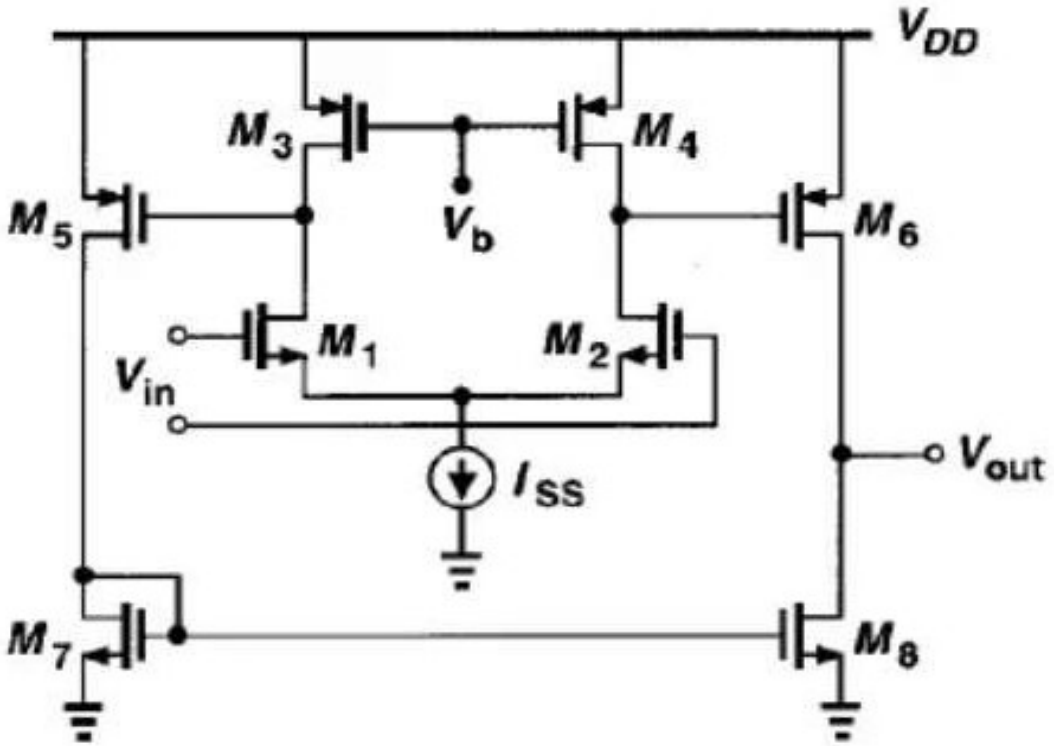
$$A_{v,\text{1st stage}} = g_{m1,2}(r_{o1,2} \parallel r_{o3,4})$$

$$A_{v,\text{2nd stage}} = g_{m5,6}(r_{o5,6} \parallel r_{o7,8})$$

Overall gain $A_v = A_{v,\text{1st stage}} \times A_{v,\text{2nd stage}}$

Output swing = $V_{DD} - |V_{OD5,6}| - V_{OD7,8}$

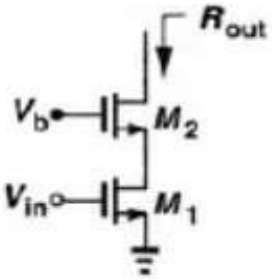
Two-stage op amp with single-ended output



Note that if the gate of M_1 is shorted to V_{out} to form a unity-gain buffer, then the minimum allowable output level is equal to $V_{GS1} + V_{ISS}$ severely limit the output swing.

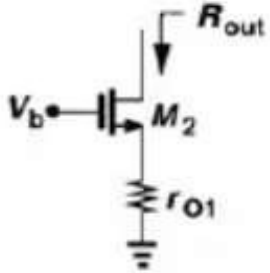
Gain boosting

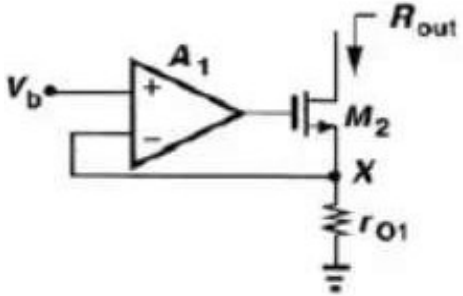
Increasing the output impedance by feedback



$R_{out} = g_{m2} r_{o2} r_{o1}$

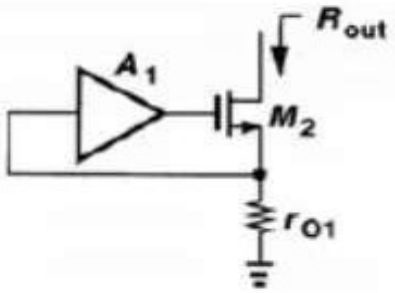
M_1 operates as a degeneration resistor.



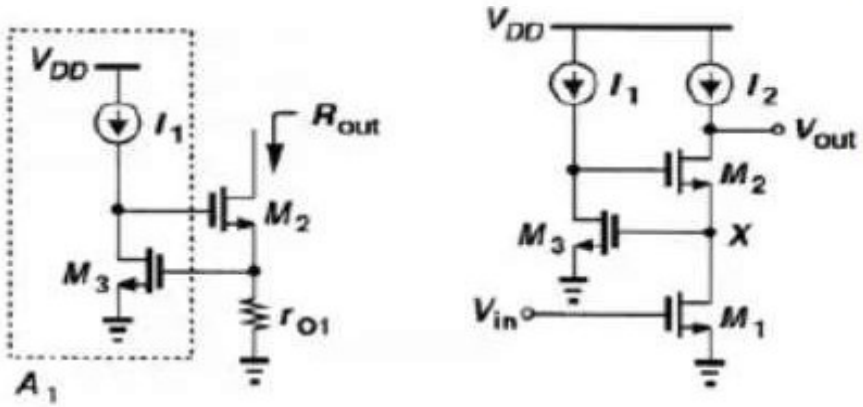


- The voltage variations at the drain of M_2 effect V_X to a lesser extent because A_1 regulates this voltage. ($V_X = V_b$) With smaller variations at X, the current through r_{o1} and hence the output current remains more constant, yielding a higher output impedance.
- $R_{out} \approx A_1 g_{m2} r_{o2} r_{o1}$,
  R_{out} is booted substantially without stacking more cascode devices on top of M_2.

Gain boosting in cascode stage



For small-signal operation, V_b is set to zero.



regulated cascode

Gain:

$$|A_v| \approx g_{m1} (g_{m2} r_{o2} r_{o1}) (g_{m3} r_{o3})$$

Min. output swing:

Since $V_X = V_{GS3}$, the min.value of V_{out} is $V_{OD2} + V_{GS3}$. The auxiliary amplifier limits the output swing.

Note: Min. output swing is $V_{OD2} + V_{OD1}$ in a simple cascode.

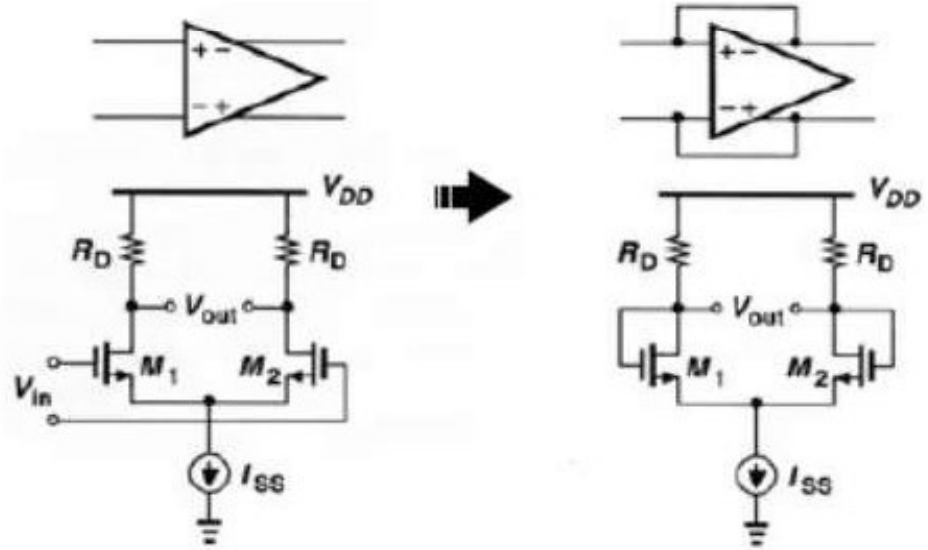
Comparison of performance of various op amp topologies

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

Common-mode feedback (CMFB)

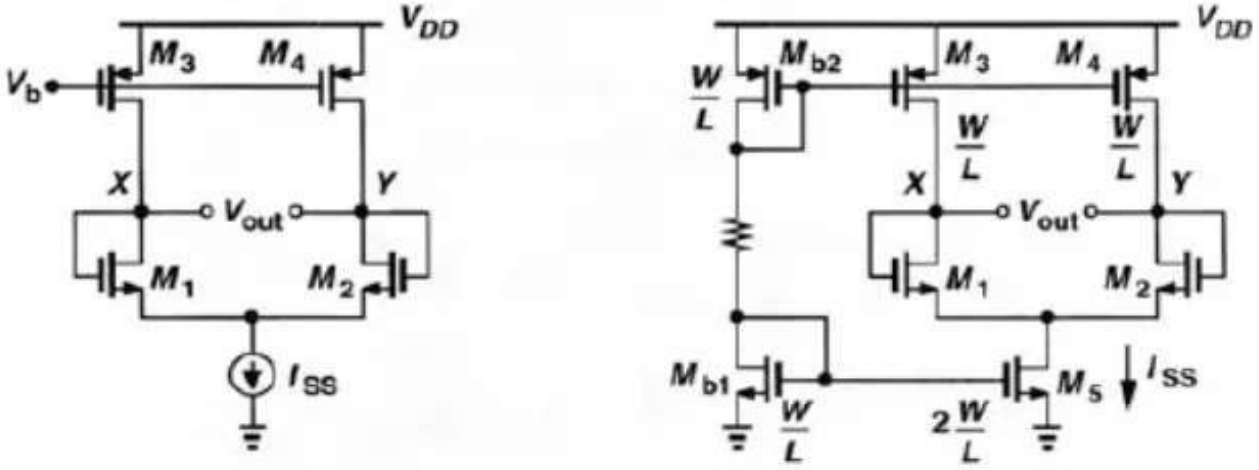
- Full differential circuits have many advantages over their single-ended counterparts such as greater output swings, avoiding mirror poles, higher closed-loop speed. However, high-gain differential circuits require *common-mode feedback*.

- Simple differential pair



Input & output common-mode level is equal to $V_{DD} - I_{SS}R_D/2$

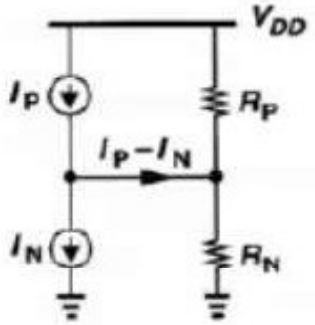
High-gain differential pair with inputs shorted to outputs



- What is the common-mode level at nodes X and Y?
  Since each of the input transistors carries a current $I_{SS}/2$, the CM level depends on how close I_{D3} and I_{D4} are to this value.
- Effect of current mismatches: Mismatches in the PMOS and NMOS current mirrors defining I_{SS} and $I_{D3,4}$ create a finite error between $I_{D3,4}$ and $I_{SS}/2$.
  If $I_{D3,4} > I_{SS}/2$, then both M_3 and M_4 must enter the triode region so that their drain currents fall to $I_{SS}/2$. Conversely, If $I_{D3,4} < I_{SS}/2$, then both V_X and V_Y must drop so that M_5 enters the triode region, thereby producing only $2I_{D3,4}$.

Simplified model of high-gain amplifier

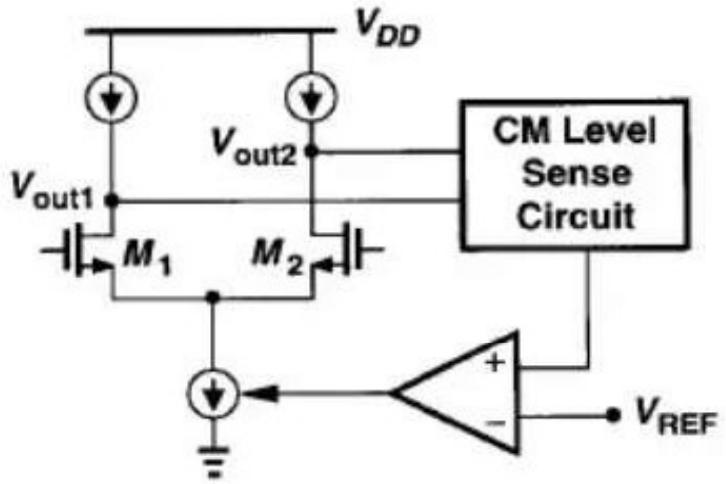
In high-gain amplifiers, we wish a *p*-type current source to balance an *n*-type current source.



$$\Delta V = (I_P - I_N)(R_P \| R_N)$$

- Since the current error depends on mismatches and $R_P \| R_N$ is quite high, the voltage error may be large, thus driving the *p*-type or *n*-type current source into triode region.
- As a general rule, if the output CM level cannot be determined by "visual inspection" and requires calculations based on device properties, then it is poorly defined.
- In high-gain amplifiers, the output CM level is quite sensitive to device properties and mismatches and it cannot be stabilized by means of differential feedback. Thus a CMFB network must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the amplifier.

Conceptual topology for CMFB



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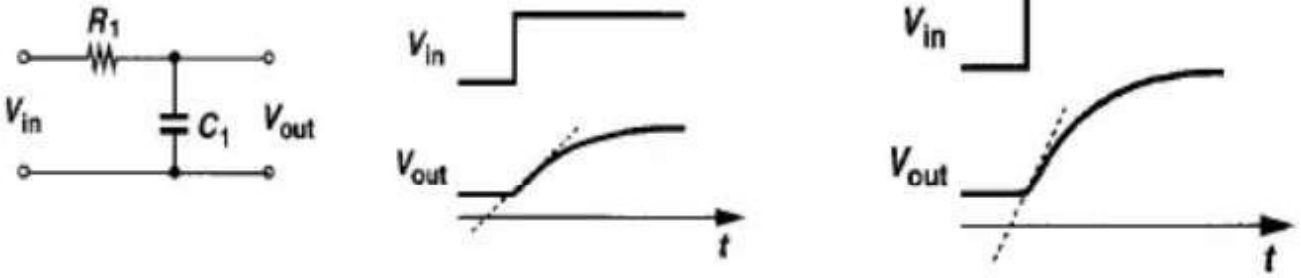
Slew rate

- Response of a linear circuit to input step



- dV_{out}/dt: Since $V_{out} = V_0[1 - \exp(-t/\tau)]$, where $\tau = RC$, we have

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\frac{-t}{\tau}$$

- $dV_{out}/dt \propto V_0$; if we apply a larger input step, the output rises more rapidly.

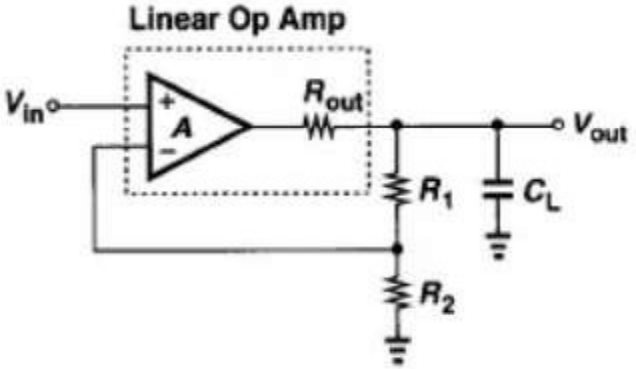
Slew rate (cont'd)

- Response of a linear op amp to step response
  - Assume op amp is linear,

$$\left[\left(V_{in}-V_{out}\frac{R_2}{R_1+R_2}\right)A-V_{out}\right]\frac{1}{R_{out}}=\frac{V_{out}}{R_1+R_2}+V_{out}C_L s$$

Assume $R_1 + R_2 >> R_{out}$, we have

$$\frac{V_{out}}{V_{in}}(s)\approx\frac{A}{\left(1+A\frac{R_2}{R_1+R_2}\right)\left[1+\frac{R_{out}C_L}{1+AR_2/(R_1+R_2)}s\right]}$$



The step response is given by

$$V_{out}=V_0\frac{A}{1+A\frac{R_2}{R_1+R_2}}\left(1-\exp\frac{-t}{\frac{C_L R_{out}}{1+AR_2/(R_1+R_2)}}\right)u(t)$$

indicating that the slope is proportional to the final value.
This type of response is called "linear settling."

- While the small-signal bandwidth of a circuit may suggest a fast time-domain response, the large-signal speed may be limited by the slew rate simply because the current available to charge and discharge the dominant capacitor in the circuit is small.

- Since the input/output relationship during slewing is nonlinear, the output of a skewing amplifier exhibits substantial distortion.

  - For example, if a circuit is to amplify a sinusoid $V_0 \sin \omega_0 t$ (in the steady state), then its slew rate must exceed $V_0 \omega_0$.

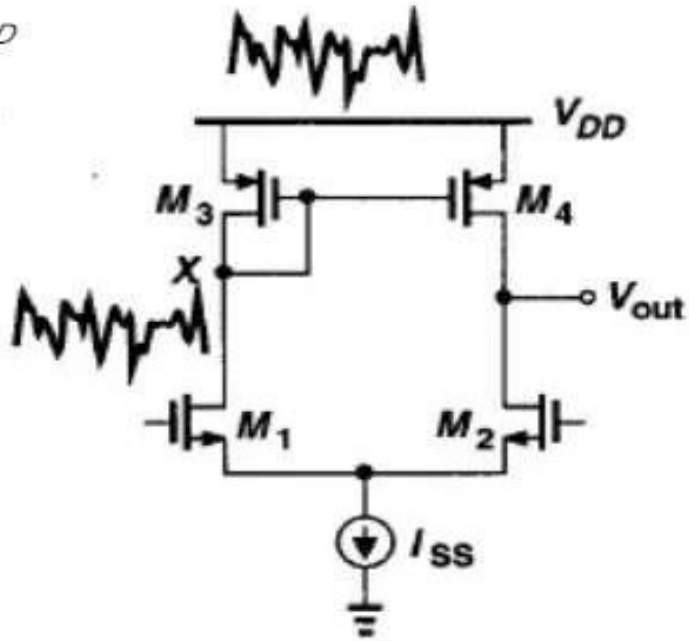
Power supply rejection

- If the circuit in the figure is perfectly symmetric, $V_{out} = V_X$. Since the diode-connected device "clamps" node X to V_{DD} V_X and hence V_{out} experience approximately the same change as does V_{DD}. In other words, the gain from V_{DD} to V_{out} is

$$\frac{\partial V_{out}}{\partial V_{DD}} \approx 1$$

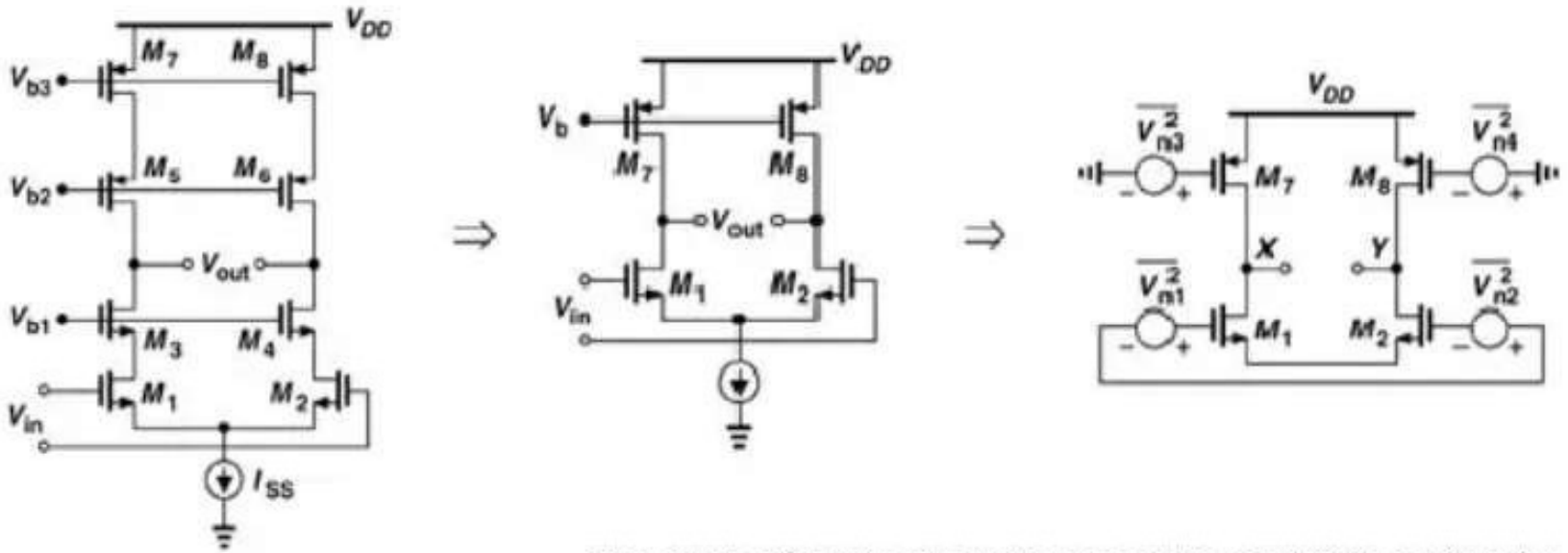
- The power supply rejection ratio (*PSRR*) is defined as the gain from the input to the output divided by the gain from the supply to the output. At low frequencies:

$$PSRR = \frac{\partial V_{out} / \partial V_{in}}{\partial V_{out} / \partial V_{DD}} \approx g_{mN}(r_{oP} \| r_{oN})$$



Noise in a telescopic op amp

- *Guide*: With many transistors in an op amp, it may seem difficult to intuitively identify the dominant sources of noise. A simple rule for inspection is to change the gate voltage of each transistor by a small amount and predict the effect at the output.



At relatively low frequency, the cascode devices contribute negligible noise, leaving M_1-M_2 and M_7-M_8 as the primary noise sources.

The input-referred noise voltage per unit bandwidth is given by

$$\overline{V_n^2} = 4kT\left(2\frac{2}{3g_{m1,2}} + 2\frac{2g_{m7,8}}{3g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\cdot\frac{g_{m7,8}^2}{g_{m1,2}^2}$$

where K_N and K_P denote the 1/f noise coefficients of NMOS and PMOS devices, respectively.

Noise in a fold-cascode op amp

- The noise of the cascode devices is negligible at low frequencies, leaving M_1-M_2, M_7-M_8, and M_9-M_{10} as potentially significant sources.
- Thermal noise:

$$\overline{V_{n,out}^2}\Big|_{M7,8} = 2\left(4kT\frac{2}{3g_{m7,8}}g_{m7,8}^2R_{out}^2\right), \text{ (uncorrelated noise)}$$

where the factor 2 accounts for noise of *M7* and *M8*, and *Rout* denotes the open-loop output resistance of the op amp.

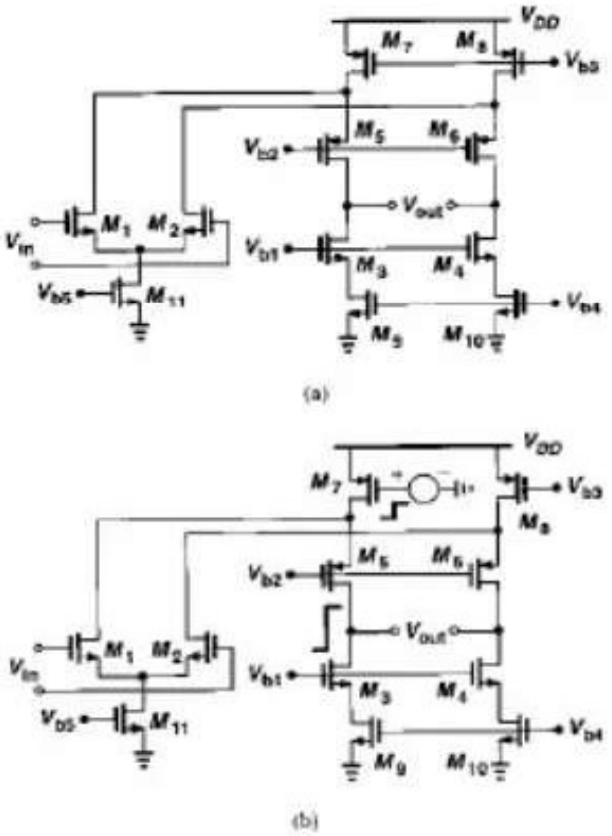
$$\overline{V_{n,out}^2}\Big|_{M9,10} = 2\left(4kT\frac{2}{3g_{m9,10}}g_{m9,10}^2R_{out}^2\right)$$

$$\overline{V_{n,out}^2}\Big|_{M1,2} = 2\left(4kT\frac{2}{3g_{m1,2}}g_{m1,2}^2R_{out}^2\right)$$

and $A_v = g_{m1,2}R_{out}$

Total input-referred thermal noise:

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out,tot}^2}}{A_v^2} = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2}{3}\frac{g_{m7,8}}{g_{m1,2}^2} + \frac{2}{3}\frac{g_{m9,10}}{g_{m1,2}^2}\right)$$



Noise in a fold-cascode op amp (cont'd)

- Flicker noise:

$$\overline{V_{n,out}^2}\Big|_{M7,8} = 2\left(\frac{K_P}{C_{ox}(WL)_{7,8}}\frac{1}{f}g_{m7,8}^2 R_{out}^2\right)$$

$$\overline{V_{n,out}^2}\Big|_{M9,10} = 2\left(\frac{K_N}{C_{ox}(WL)_{9,10}}\frac{1}{f}g_{m9,10}^2 R_{out}^2\right)$$

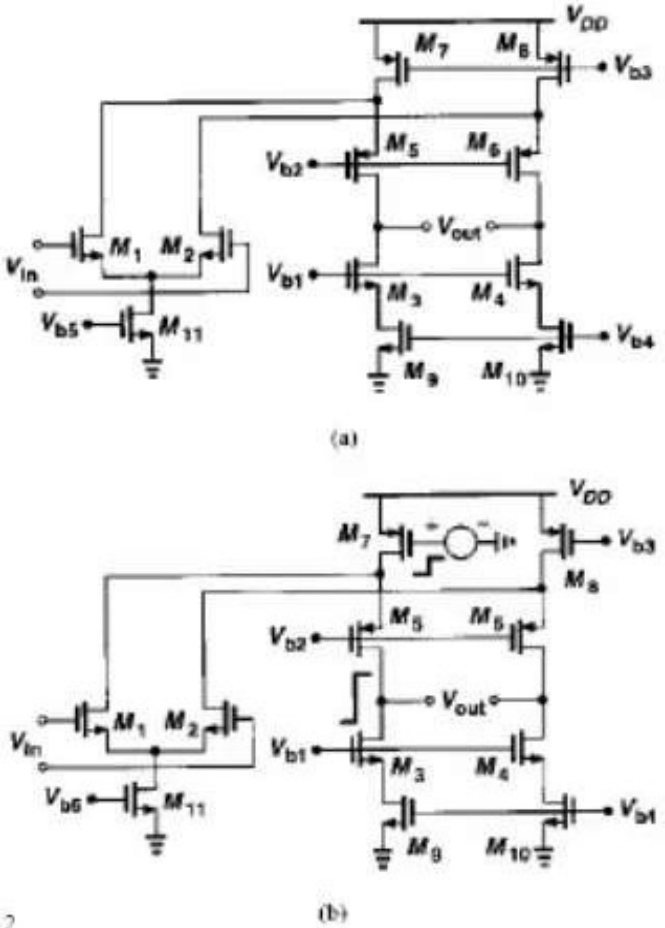
$$\overline{V_{n,out}^2}\Big|_{M1,2} = 2\left(\frac{K_N}{C_{ox}(WL)_{1,2}}\frac{1}{f}g_{m1,2}^2 R_{out}^2\right)$$

and $A_V = g_{m1,2}R_{out}$.

Total input-referred flicker noise:

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out,tot}^2}}{A_v^2}$$

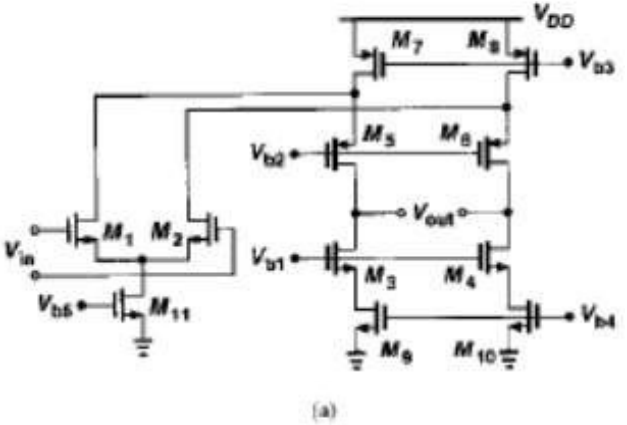
$$= \frac{2K_N}{C_{ox}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{9,10}}\frac{g_{m9,10}^2}{g_{m1,2}^2}\right) + \frac{2K_P}{C_{ox}f}\frac{1}{(WL)_{7,8}}\frac{g_{m7,8}^2}{g_{m1,2}^2}$$



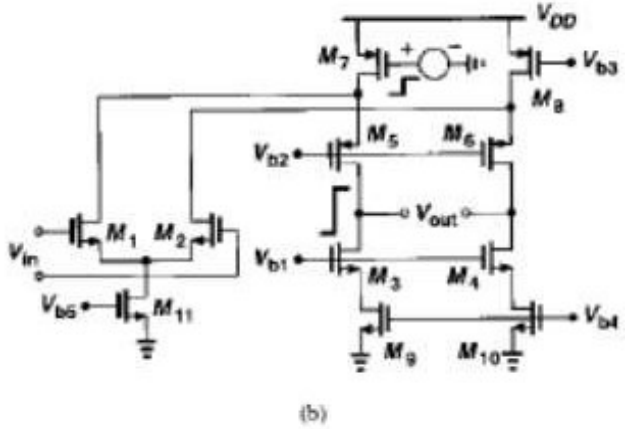
Noise in a fold-cascode op amp (cont'd)

- The overall noise:

$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2}{3}\frac{g_{m7,8}}{g_{m1,2}^2} + \frac{2}{3}\frac{g_{m9,10}}{g_{m1,2}^2}\right) + \frac{2K_N}{C_{ox}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{9,10}}\frac{g_{m9,10}^2}{g_{m1,2}^2}\right) + \frac{2K_P}{C_{ox}f}\frac{1}{(WL)_{7,8}}\frac{g_{m7,8}^2}{g_{m1,2}^2}$$



(a)



(b)

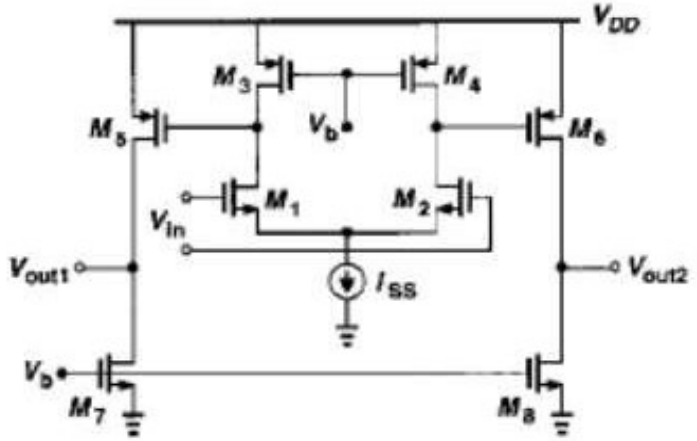
- Discussion:
  - The noise contribution of the PMOS and NMOS current sources *increases* in proportion to their transconductance. This trend results in a trade-off between output voltage swings and input-referred noise: for a given current, as implied by $g_m = 2I_D/(V_{GS} - V_{TH})$, if the overdrive voltage of the current sources is minimized to allow large swings, then their transconductance is maximized.

Noise in a two-stage op amp

- Total voltage gain: $A_v = g_{m1}(r_{o1} \| r_{o3}) \times g_{m5}(r_{o5} \| r_{o7})$.
- In the 2nd stage: The noise current of *M*5 and *M*7 flows through *ro*5||*ro*7.

$$\overline{V_n^2}\Big|_{M_{5-8}} = 2 \times 4kT\frac{2}{3}(g_{m5}+g_{m7})(r_{o5} \| r_{o7})^2 \cdot \frac{1}{A_v^2} = \frac{16kT}{3}\frac{g_{m5}+g_{m7}}{g_{m1}^2 g_{m5}^2 (r_{o1} \| r_{o3})^2}$$

- In the 1st stage: $\overline{V_n^2}\Big|_{M_{1-4}} = 2 \times 4kT\frac{2}{3}\frac{g_{m1}+g_{m3}}{g_{m1}^2}$
- Total input-referred thermal noise: $\overline{V_{n,tot}^2} = \frac{16kT}{3}\frac{1}{g_{m1}^2}\left[g_{m1}+g_{m3}+\frac{g_{m5}+g_{m7}}{g_{m5}^2(r_{o1} \| r_{o3})^2}\right]$



- Note the noise resulting from the second stage is usually negligible because it is divided by the gain of the first stage when referred to the main input.